Stability Assessment of Fixed Regulators

Tom Boehler - Senior Design and Test Specialist
Paul Ho - Senior Engineering Scientist

There are cases where a Bode (gain-phase) plot cannot be obtained from a control loop. For example, a three terminal regulator or hybrid may not have its control loop exposed. With integrated production hardware, it may not be possible to break into the control loop and inject a signal. In these cases the stability may still be determined by testing or simulating the circuit's output impedance. This includes the stability of control loops associated with power supply circuits and opamps, regardless if the circuit is being bench tested or simulated in SPICE. Both bandwidth and phase margin can be determined from output impedance by observing peaking in the group delay of the impedance. [i]

Group delay is the time distortion between two signals (the two signals in this case being the perturbated load current and resulting voltage response) and is obtained by differentiating the phase difference between the current and the voltage. Group delay is defined as:

$$Tg = \frac{d\phi}{d\omega}$$

This derivation can be easily made to the phase curve using the post-processing program found in most SPICE software suites. Once the group delay curve has been plotted, peaking in the curve is indicative of a rapid phase transition. Rapid phase transitions occur primarily in two cases:

1. There is an LC resonance from a filter or self-resonance of an inductor or capacitor
2. The zero crossing of a single-order system's loop gain.

Each peak in the group delay represents a unique Quality Factor or "Q" and these peaks can present themselves as voltage oscillations with dynamic load currents at the frequency of the peak. The higher the Q of each peak, the more susceptible the circuit is to oscillations at that peak's frequency. Q is defined as:

$$Q = Tg \cdot Freq \cdot \pi$$

where Tg is the group delay value at a given peak on the curve and Freq is the frequency of the peak.[ii] From this Q value, we can compute the exact phase margin value.

It is more fitting to simply define the phase margin as the "stability margin" as it is not always the measure of the phase distance from zero at the gain zero crossing frequency. Nyquist plots are used to evaluate closed-loop stability by plotting the gain-phase vector (of the output impedance in this case) in Cartesian coordinates where the real part of the impedance is on the X-axis and the imaginary portion is on the Y-axis. The minimum distance between the plotted vector and the point (1,0) defines the stability of the system. [iii] For example, in a system where the gain and phase intersect the point (1,0) in the

Nyquist plot, this is defined as a perfect oscillator (Q approaches infinity). Phase margin or, stability margin is, therefore, defined as:

$$PM(T_g, f) := -180 \cdot \frac{\operatorname{atan2}\left[\frac{1}{4\cdot\pi^2}\cdot\frac{2\cdot\pi^2\cdot f\cdot T_g - 2\cdot\pi + 2\cdot\left(\pi^4\cdot f^2\cdot T_g^{\,2} + 2\cdot\pi^3\cdot f\cdot T_g - \pi^2\right)^{\frac{1}{2}}}{T_g\cdot f},\ \frac{\pi\cdot f\cdot T_g - \frac{1}{4\cdot\pi}\cdot\left[2\cdot\pi^2\cdot f\cdot T_g - 2\cdot\pi + 2\cdot\left(\pi^4\cdot f^2\cdot T_g^{\,2} + 2\cdot\pi^3\cdot f\cdot T_g - \pi^2\right)^{\frac{1}{2}}\right] - 1}{\pi\cdot f\cdot T_g}\right]}{\pi}$$

By looking at the output impedance of a regulator we can extract a phase margin value to assess the stability of our system. Alternate methods to extract stability information such as load stepping do not quantitatively define loop stability and are **not** recommended for stability analysis, though load stepping can be one of many qualitative stability indicators. A quantifiable phase margin value is often needed in cases where end-of-life or beginning-of-life performance requirements must be met.

For instance, worst case analysis guidelines for Space applications specify a minimum of 30 degrees phase margin at end-of-life Stability can ONLY be assessed in SPICE, or other RF/analog simulation tool, where tolerances can be applied to the circuit. In addition, the IC itself model MUST be toleranced as the bandwidth, open loop gain variations, and other aspects of the IC that interact with the load impedance and impact the stability result.

Beginning-of-life phase margin testing is not sufficient to preclude the need for EOL WCCA. Experience indicates that there is often a 20 degree reduction in phase margin, or more, possible from BOL to EOL due to various tolerances. In addition, some regulators have an irregular phase response with dips that greatly exacerbate the BOL to EOL shift. Therefore, WCCA is a necessity on all regulators.

Testing over temperature can provide a limited BOL assessment. A full worst case analysis is the only way that regulator and converter stability performance can be accurately quantified over the life of the product.

Simulating Output Impedance

In order to simulate the output impedance of a regulator, an AC current source needs to be added from its output to ground. Plotting the voltage of the regulator output is equivalent to plotting its output impedance if the AC magnitude of the current source is 1. The voltage magnitude and group delay need to be plotted in order to determine the stability from the regulator's output impedance.

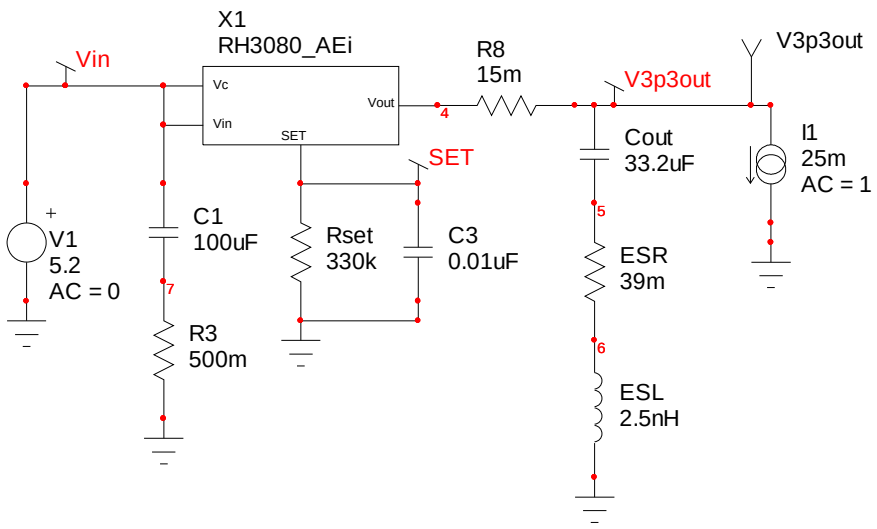

Figure 1: The regulator circuit simulation set up to measure the output impedance. Note that the DC current source and the AC current source can be combined into one current source.

To determine the correct value of group delay to measure, the absolute value of the group delay curve is plotted using a logarithmic scale. Next, locate the peak of the group delay from the plot. You can also plot the magnitude of the impedance using a logarithmic scale, or the dB magnitude, of the impedance. This can aid in determining the correct peak in the group delay plot as it coincides with either a local maxima or minima in the magnitude of the impedance.

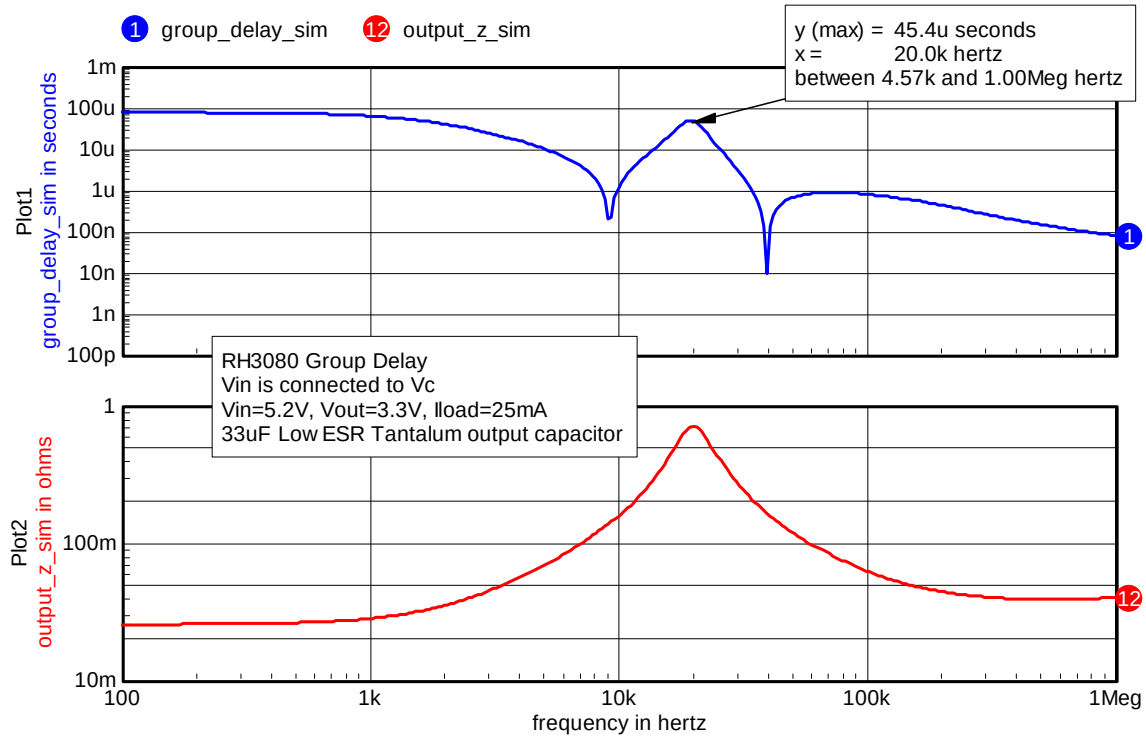

Figure 2: Plot of the simulated output impedance and group delay of the test circuit.

Using the group delay value and frequency of the peak seen in both the group delay and impedance plots, we can extract the bandwidth, Q and phase margin of the circuit.

$$Q\left(45.4\cdot 10^{-6}, 20\cdot 10^{3}\right) = 2.853$$

$$PM\left(45.4\cdot 10^{-6}, 20\cdot 10^{3}\right) = 19.875$$

The bandwidth and phase margin of this particular circuit are 20 kHz and 20 degrees, respectively.

Measuring Output Impedance

Output impedance can be bench tested and is best done so on the actual production hardware using the same methodology used for simulating the output impedance.

The equipment that is needed includes:

- Network Analyzer (VNA) that plots group delay
- Current Injector (Picotest J2111A for example)
- 1:1 Voltage Probe

Figure 3: Image showing the Picotest J2111A Current Injector and OMICRON Lab Bode 100 VNA connected to the regulator under test.[iv]

Following the connection diagram shown below, connect the 1:1 voltage probe and the output of the Current Injector to the output of the regulator or other device under test (both with respect to ground).

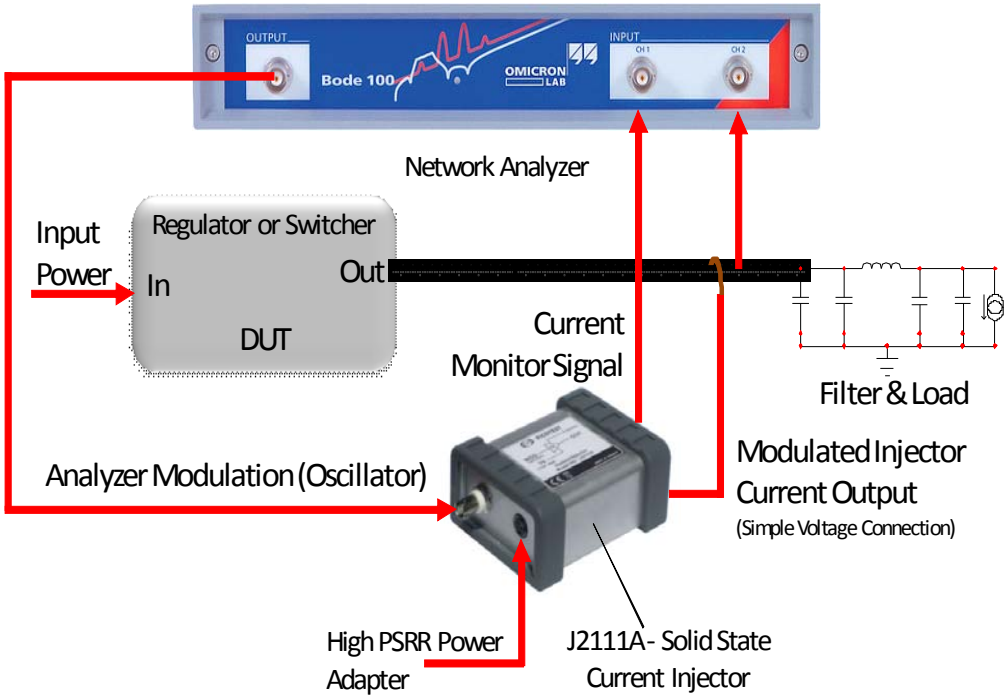

Figure 4: Current Injector and Network Analyzer connection diagram for output impedance measurements.

Figure 4 shows the basic measurement setup to measure the output impedance of a regulator. The output of the network analyzer is connected to the modulation input of the Current Injector. A signal at the input of the injector leads to a change in load current. For the J2111A, in particular, the input-output signal has gain of 10mA/V.

The monitor output of the injector then delivers a voltage signal that is proportional to the current flowing through the injector output ($1\mathrm{A} = 1\mathrm{V}$). This signal is measured at channel 1. The output voltage is then measured at channel 2 using the 1:1 probe. Performing a gain measurement of this connection results in the output impedance:

$$\frac{V_{ch2}}{V_{ch1}} \triangleq \frac{V_{out}}{I_{out}} \triangleq Z_{out}$$

	Frequency	Trace 1		Trace 2	
Cursor 1	19.133 kHz		663.535 m		40.224 µs
Cursor 2					
delta C2-C1					
Phase Margin C1	19.133 kHz			2.418	22.613 °

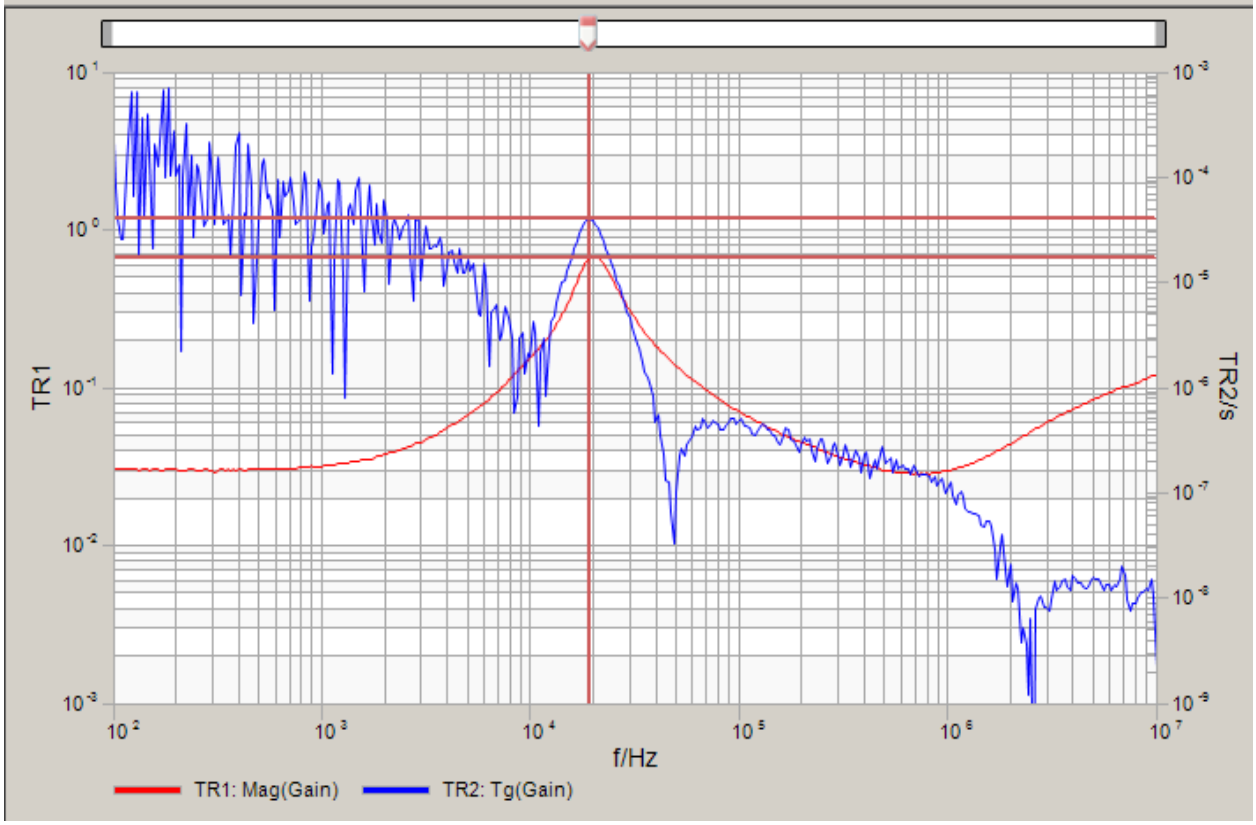

Figure 5: Plot of the measured output impedance of a test circuit. Resulting bandwidth, Q and phase margin are 19 kHz, 2.418 and 23 degrees, respectively.

The math required to extract the Q and phase margin from the group delay curve is integrated into the Bode 100 VNA software making stability assessment a simple cursor measurement.

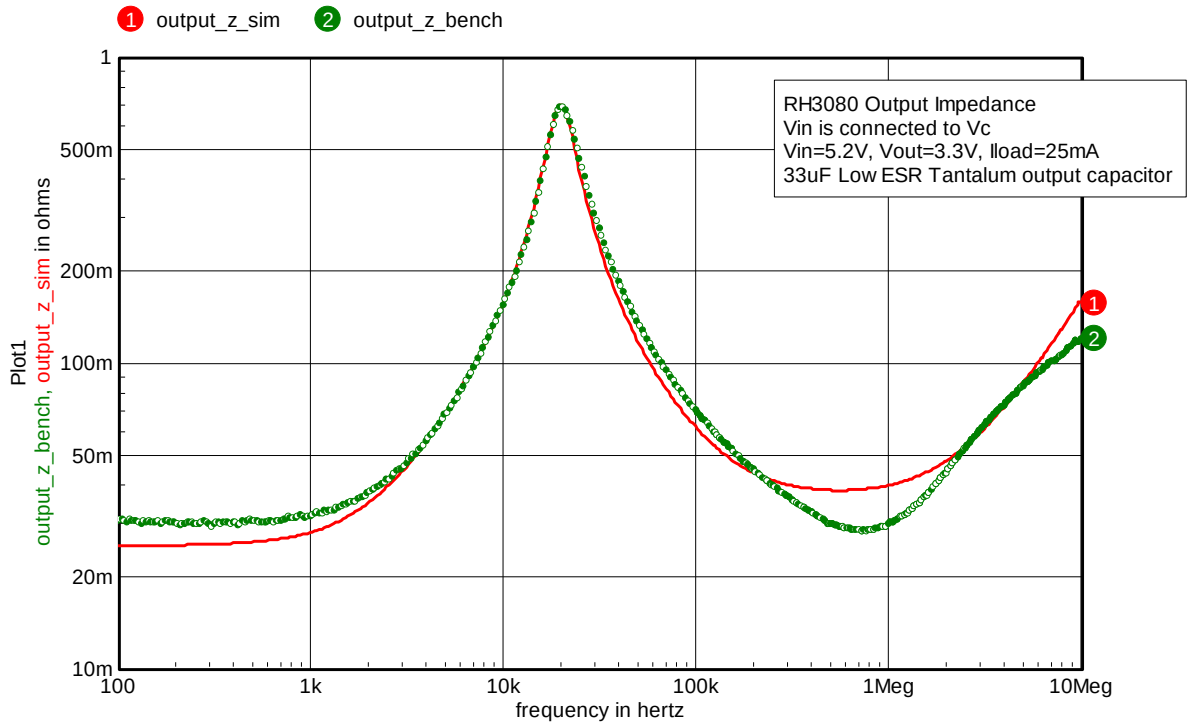

Figure 6: Bench-simulation overlay of the simulated and measured output impedance magnitude.

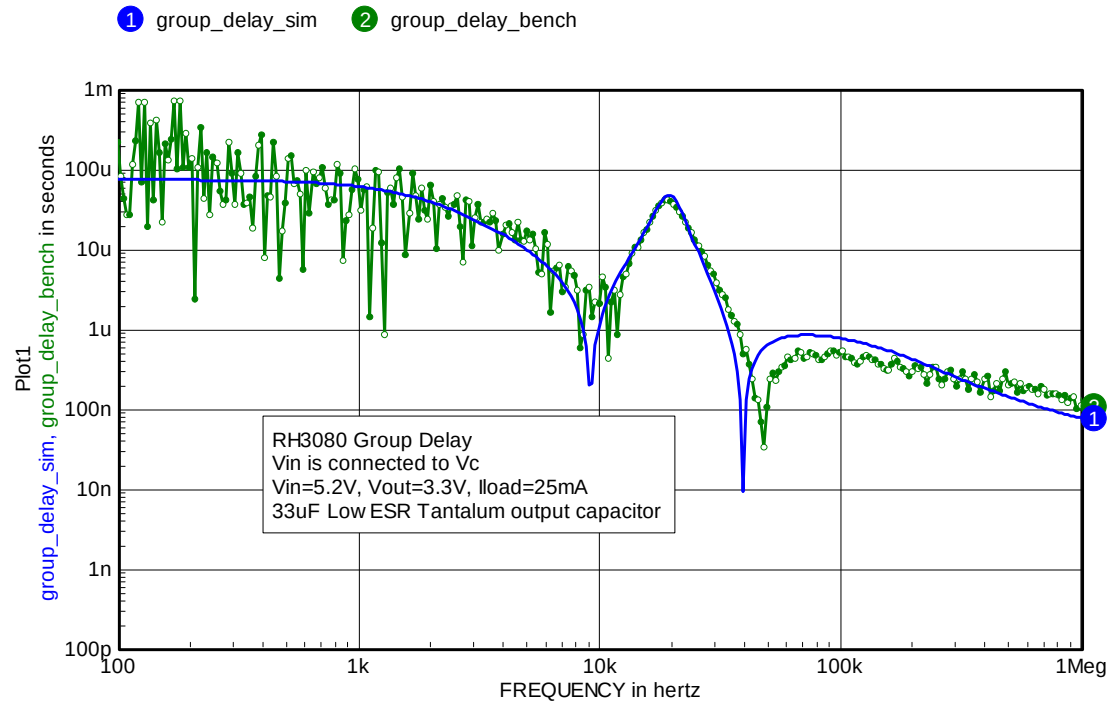

Figure 7: Bench-simulation overlay of the simulated and measured group delay.

The bench and simulated bandwidth and phase margin of the RH3080 are in excellent agreement. This measurement technique can be used for filters, linear regulators, switching regulators, op-amps and other circuitry where assessing stability is relevant. For more information on measuring stability and using Signal Injectors, please visit https://www.picotest.com/blog/ for various articles discussing this topic and more.

---

[i] "New Technique for Non-Invasive Testing of Regulator Stability", Steven Sandler and Charles Hymowitz, Power Electronics Technology, September 2011

[ii] Erickson, Robert W. and Maksimovic, Dragan. Fundamentals of Power Electronics. s.l.: Springer, 2004.

[iii] "When Bode Plots Fail Us", Steve Sandler, Paul Ho, and Charles Hymowitz, AEi Systems, White Paper, http://www.aeng.com/design_analysis.htm, February 2012

[iv] OMICRON Lab. www.omicron-lab.com/application-notes. Measurement of DC/DC converters with Bode 100. [Online] 2009.