

Characterizing and Selecting the VRM

Steven M. Sandler, (Picotest)

Paper Steve M. Sandler (Picotest)

DESIGNCON 2017
WHERE THE CHIP MEETS THE BOARD



JAN 31-FEB 2, 2017



Characterizing and Selecting the VRM

Steven M. Sandler, (Picotest)

Paper Steve M. Sandler (Picotest)

DESIGNCON® 2017
WHERE THE CHIP MEETS THE BOARD



JAN 31-FEB 2, 2017



The Big Issues

VRMs and VRM controllers are often poorly characterized providing limited, poor quality, or incorrect data

Figures of Merit are limited to a few general characteristics (i.e. voltage accuracy, efficiency, size)

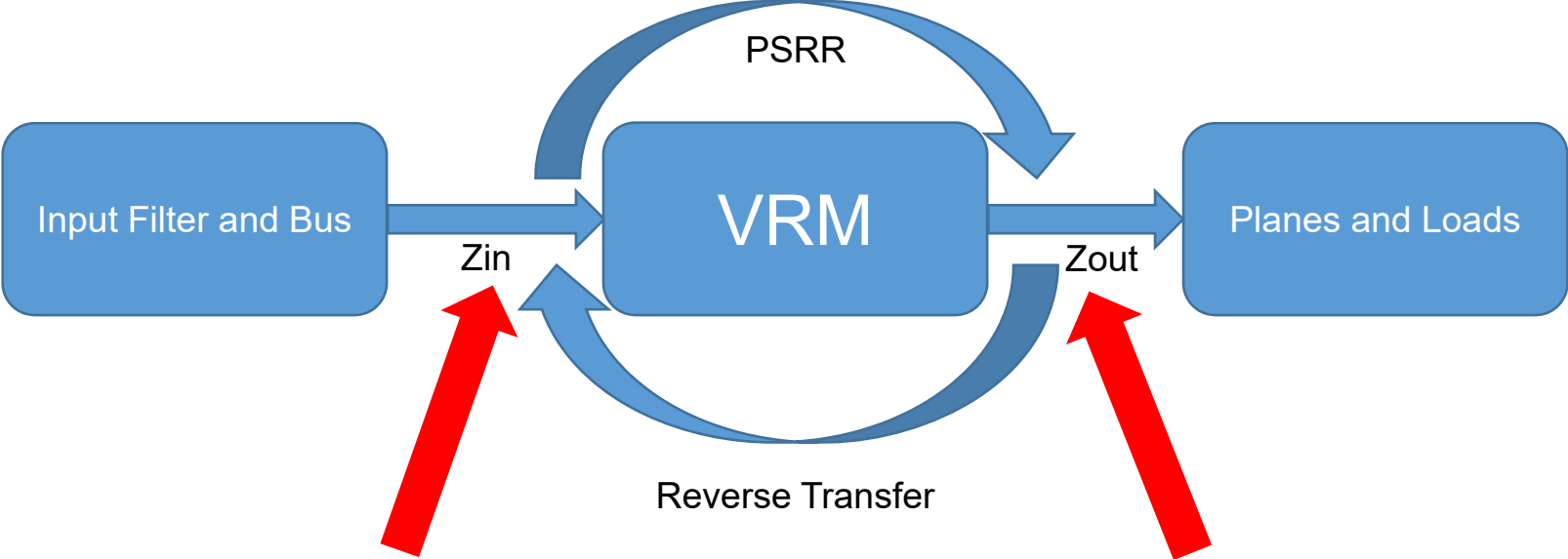
In many cases, reference designs and manufacturer recommendations are **poor or inappropriate**

Evaluation boards are not constructed to support precise measurement or modification

In this session, we will define key VRM characteristics and provide tips on how to select one. We'll also show potential issues to look out for



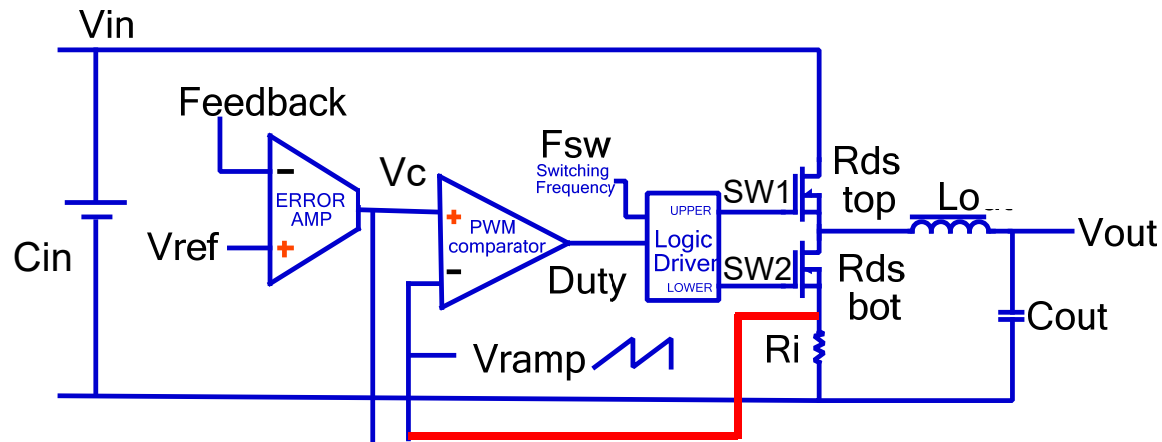
Small Signal System Interfaces



Stability concerns exist at both the input and the output

Unified State Space Average Model

Voltage Mode and **Current Mode**



The current mode control topology differs from the voltage mode topology **by the addition of a signal related to the inductor current.**

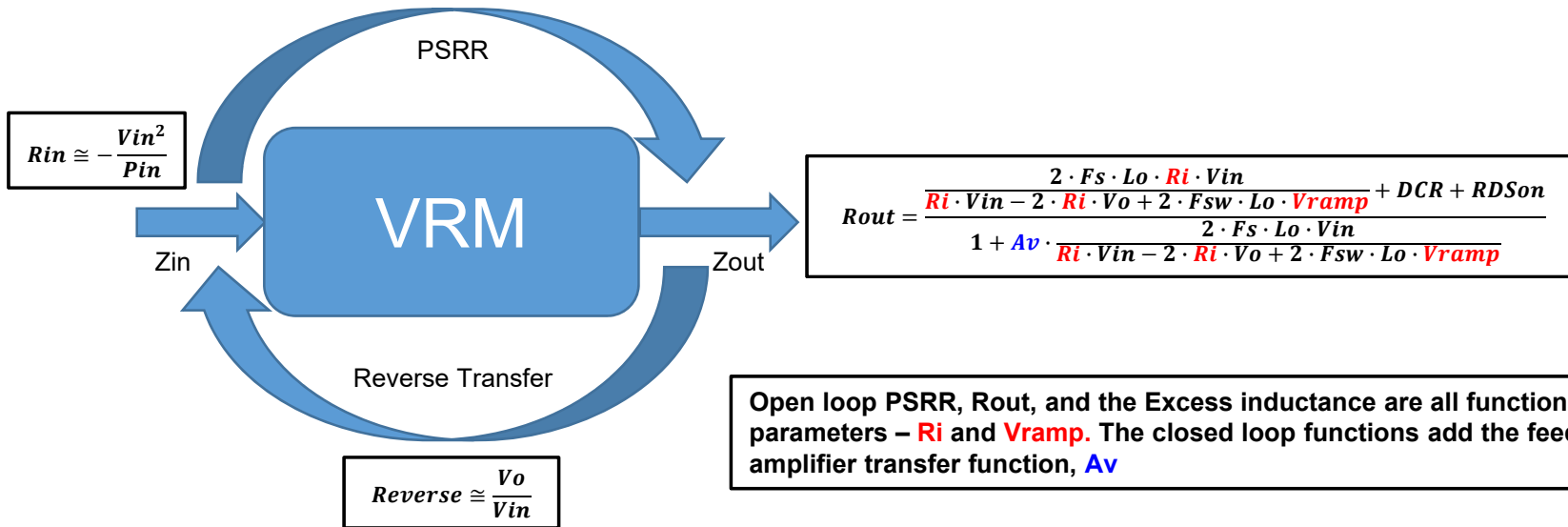
A model that includes both the current signal and the ramp signal, with the ability to proportion them, supports both modes of operation.

This unified model gives us a complete perspective of the operation and allows optimization of these common VRM topologies (and/or lack thereof)



Small Signal Responses (State Space Averaged)

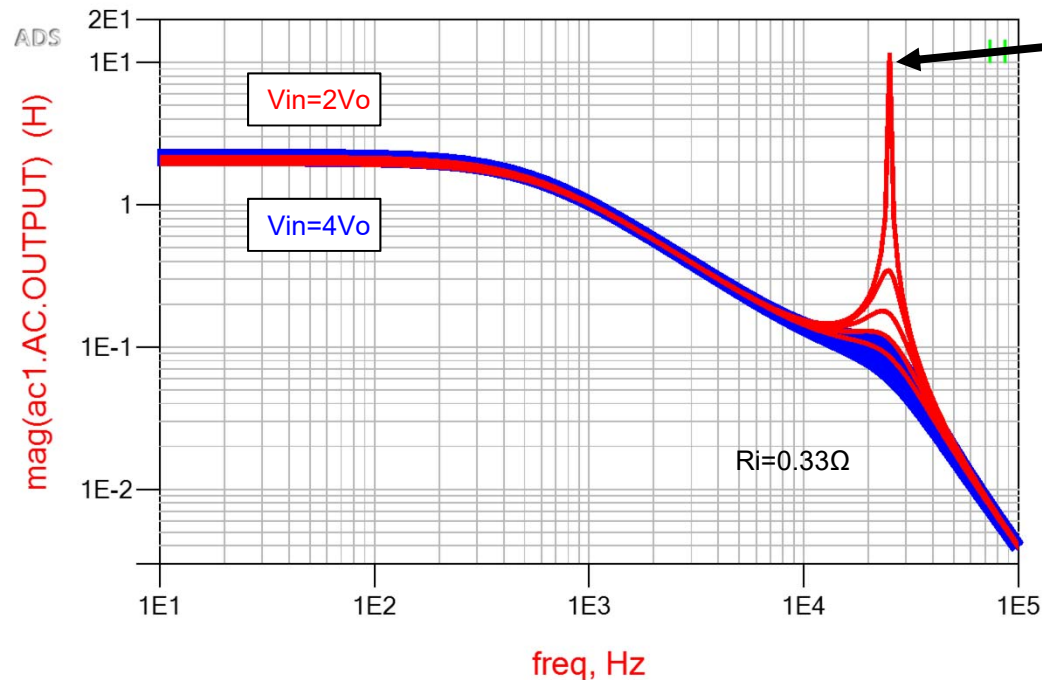
$$PSRR_{dB} = 20 \log \left| \frac{V_o \cdot (R_i \cdot V_o - 2 \cdot F_s \cdot L_o \cdot V_{ramp})}{R_i \cdot V_{in}^2 - 2 \cdot R_i \cdot V_o \cdot V_{in} + 2 \cdot F_s \cdot L_o \cdot V_{in} \cdot V_{ramp} + 2 \cdot A_v \cdot F_s \cdot L_o \cdot V_{in}} \right|$$



Open loop PSRR, R_{out} , and the Excess inductance are all functions of two parameters – R_i and V_{ramp} . The closed loop functions add the feedback amplifier transfer function, A_v

R_{in} and Reverse are less dependent, so less attention is warranted (for now)

Current Mode Subharmonic Resonance



0.000
0.125
0.250
0.375
0.500

Vramp (V)

$$M_c = 1 + \frac{F_s \cdot L_o \cdot V_{ramp}}{R_i \cdot (V_{in} - V_o)}$$

Optimizing Vramp

$$V_{ramp} = \frac{R_i (V_o - V_{in})}{F_s \cdot L_o \cdot Q} \cdot \frac{0.3183 + 0.5 \cdot Q}{\frac{V_o}{V_{in}} - 1} + Q$$

Most current modes show a high Q series resonance in the current loop near 50% duty cycle.

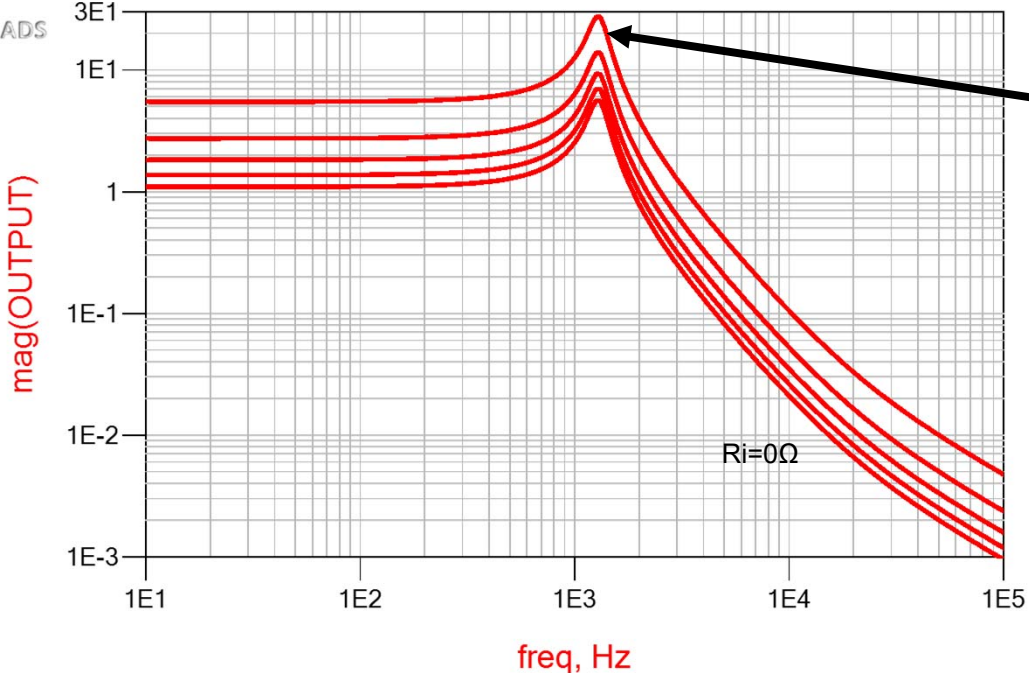
This Q is damped by the addition of a Vramp signal

$$\text{Control to Output} = \frac{2 \cdot F_s \cdot L_o \cdot V_{in}}{R_i \cdot V_{in} - 2 \cdot R_i \cdot V_o + 2 \cdot F_s \cdot L_o \cdot V_{ramp}}$$



Voltage Mode Filter Resonance

This resonance is shifted by external bulk capacitors



2
4
6
8
10

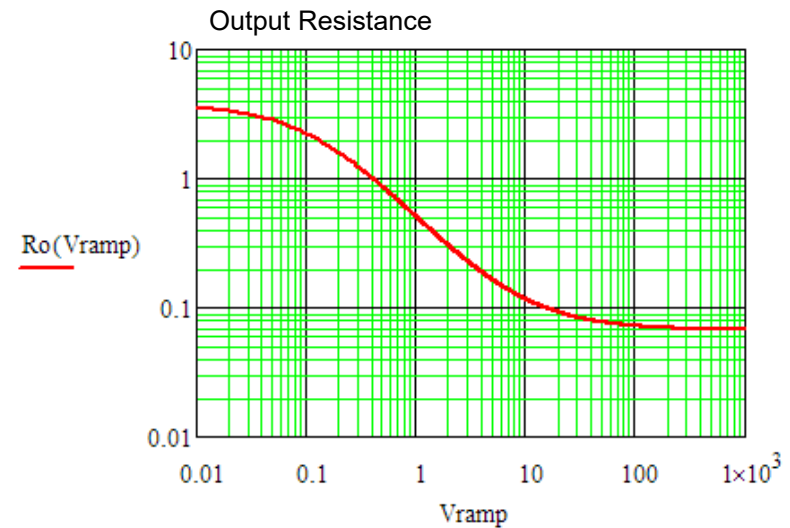
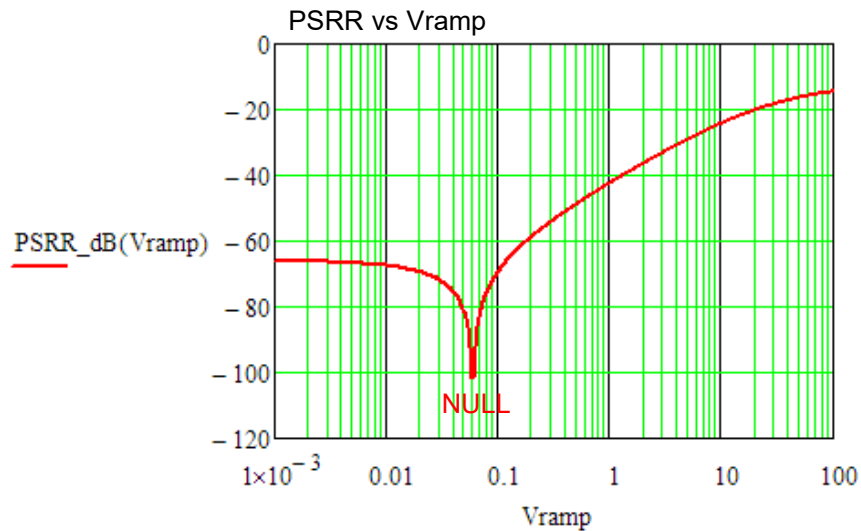
Vramp (V)

$$M_c = 1 + \frac{F_s \cdot L_o \cdot V_{ramp}}{R_i \cdot (V_{in} - V_o)} = \infty$$

Voltage modes show a high Q resonance in the voltage loop independent of duty cycle. This resonance is due to the output inductor and output capacitors

This Q is damped by the addition of the current signal

Low Frequency Open Loop PSRR and Rout



$$PSRR = \frac{V_o \cdot R_i \cdot V_o - 2 \cdot F_s \cdot L_o \cdot Vramp}{R_i \cdot Vin^2 - 2 \cdot R_i \cdot V_o \cdot Vin + 2 \cdot F_s \cdot L_o \cdot Vin \cdot Vramp}$$

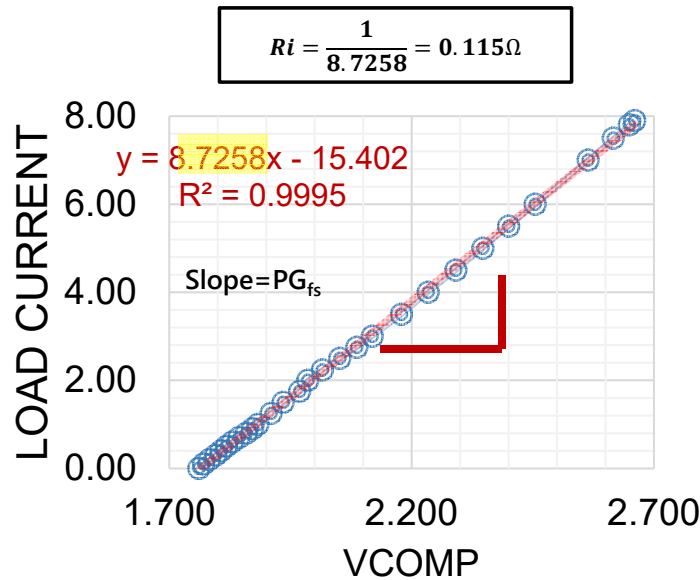
NULL

$$Vramp = \frac{R_i \cdot V_o}{2 \cdot F_s \cdot L_o}$$

$$R_{out} = \frac{\frac{2 \cdot F_s \cdot L_o \cdot R_i \cdot Vin}{R_i \cdot Vin - 2 \cdot R_i \cdot V_o + 2 \cdot F_{sw} \cdot L_o \cdot Vramp} + DCR + RD_{son}}{1 + A_v \cdot \frac{2 \cdot F_s \cdot L_o \cdot Vin}{R_i \cdot Vin - 2 \cdot R_i \cdot V_o + 2 \cdot F_{sw} \cdot L_o \cdot Vramp}}$$



Clearly Ri and Vramp are Both Critical



The measured value of R_i is 12% higher than expected due to DC PCB resistance despite the very short connections

LM25116 EVAL



$$R_i = A_{cs} \cdot R_{cs} = 0.1\Omega$$

Many controllers don't specify the Vramp characteristics at all, some do, though are not optimum, many offer less than this LM20143 except

“What makes the LM20143 unique is the amount of slope compensation will change depending on the output voltage. When operating at high output voltages the device will have more slope compensation than when operating at lower output voltages. This is accomplished in the LM20143 by using a non-linear parabolic ramp for the slope compensation.”



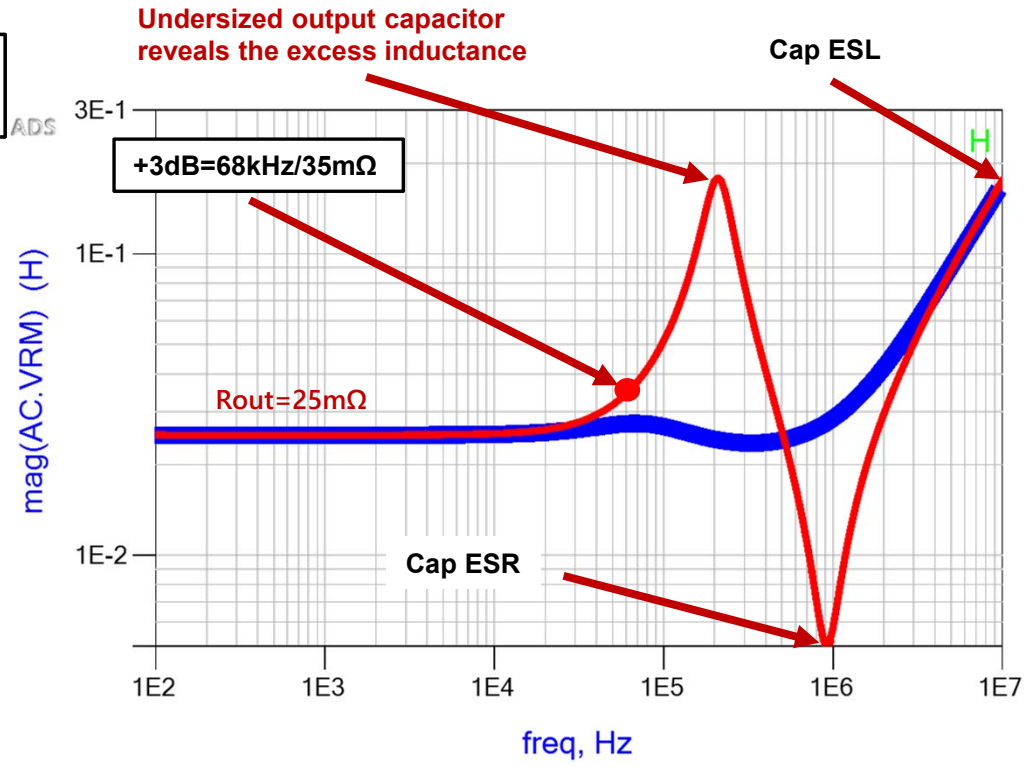
Output Inductance

$$L_{excess} = \frac{L_o}{1 + \frac{R_i \cdot V_{in} - 2 \cdot R_i \cdot V_o + 2 \cdot F_s \cdot L_o \cdot V_{ramp}}{2 \cdot F_s \cdot L_o \cdot V_{in}}} \cdot A_v + \frac{R_o}{2 \cdot \pi \cdot GBW}$$

The output inductance can best be directly measured by installing an undersized output bulk capacitor

$$L_{excess} = \frac{25m\Omega}{2\pi \cdot 68kHz} = 58.5nH$$

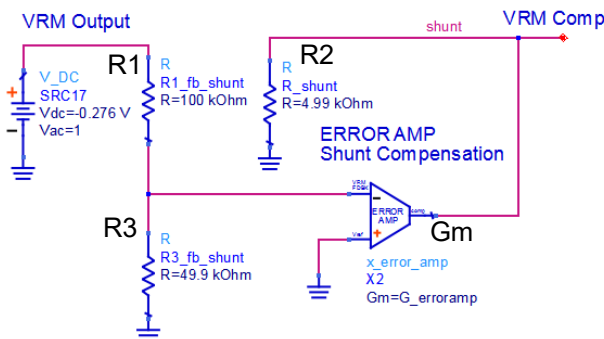
Lower inductance requires smaller output capacitors



Feedback Amplifiers

Many new devices use transconductance type error amplifiers

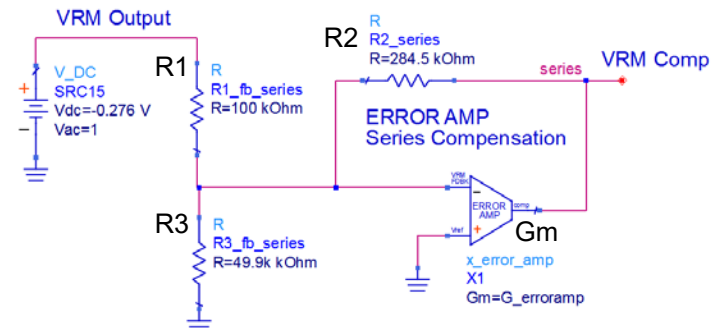
Manufacturer Suggested



$$A_{v_shunt} = \frac{R3 \cdot Gm \cdot R2shunt}{R1 + R3} = 3.215$$

$$\frac{\delta A_{v_shunt}}{\delta Gm} = \frac{R3 \cdot R2shunt}{R1 + R3} = 6.3 \cdot 10^3$$

Greatly Improved



$$A_{v_series} = \frac{R3 \cdot (Gm \cdot R2 - 1)}{R1 + R3 + Gm \cdot R1 \cdot R3} = 3.215$$

$$\frac{\delta A_{v_series}}{\delta Gm} = \frac{R2 \cdot R3}{R1 + R3 + Gm \cdot R1 \cdot R3} - \frac{R1 \cdot R3^2 \cdot (Gm \cdot R2 - 1)}{(R1 + R3 + Gm \cdot R1 \cdot R3)^2} = 2.58 \cdot 10^3$$

Higher resistor values reduce this sensitivity

Gm tolerances are often poorly specified and tolerances can be very large. The manufacturer suggested feedback is often much more sensitive to this unspecified, large tolerance (aka **BAD ADVICE**).



Feedback Amplifier Data

MAX16932

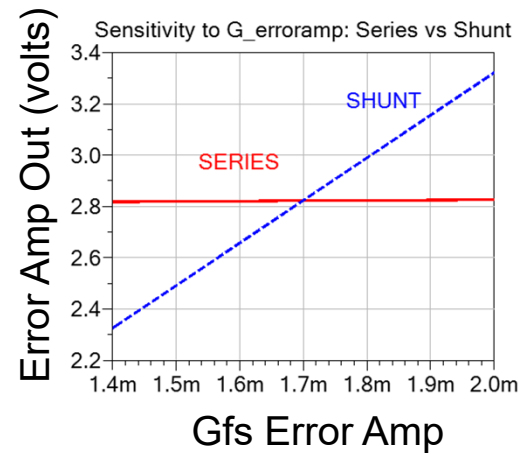
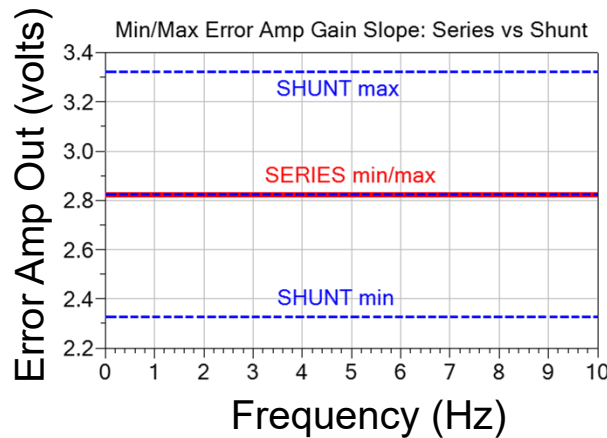
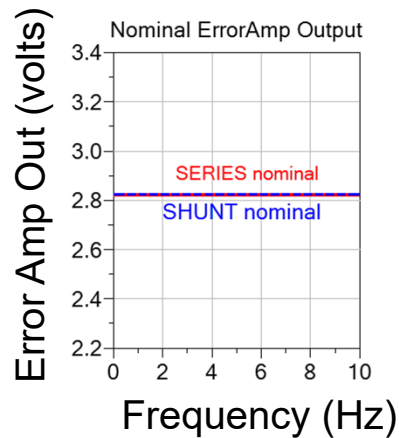
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Regulated Feedback Voltage	$V_{FB1,2}$		0.99	1.0	1.01	V
Feedback Leakage Current	$I_{FB1,2}$	$T_A = +25^\circ\text{C}$		0.01	1	μA
Feedback Line Regulation Error		$V_{IN} = 3.5\text{V to }36\text{V}, V_{FB} = 1\text{V}$		0.001		%/V
Transconductance (from FB_ to COMP_)	g_m	$V_{FB} = 1\text{V}, V_{BIAS} = 5\text{V}$		1200	2400	μS

Does this suggest the minimum is 0?

MIC2199

Error Amplifier						
Transconductance Error Amplifier GM				0.2		mS

What about other parameters such as Gain Bandwidth? Source/Sink Current?



Gfs Error Amp

Min = 1.4 e-3
 Nominal = 1.7 e-3
 Max = 2.0 e-3

Measurements Offer Access To the Unknowns

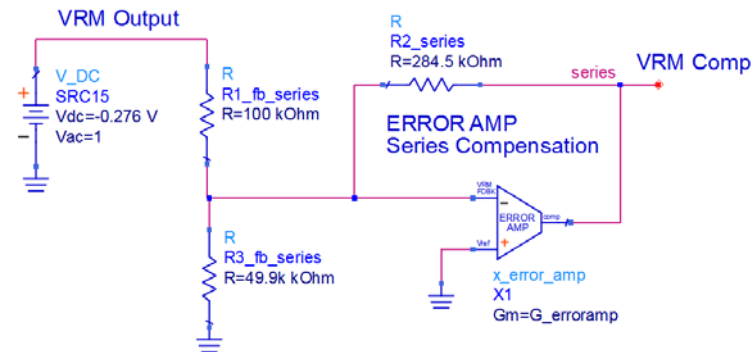
PSRR and Rout are both dependent on V_{ramp} and Ri. A PSRR measurement and an Rout measurement provide two equations for the two unknowns, which is solvable

Output effective inductance is dependent on V_{ramp}, Ri, and Av, which is further dependent on the error amplifier characteristics Gm and Gbw

$$A_v = \frac{VRM_Comp}{VRM_Output} = \frac{R_3 \cdot (G_m \cdot R_2 - 1)}{R_1 + R_3 + G_m \cdot R_1 \cdot R_3}$$

$$G_m = \frac{R_3 + A_v \cdot (R_1 + R_3)}{R_3 \cdot (R_2 \cdot A_v \cdot R_1)}$$

Unknown small signal error amplifier characteristics, Gbw and Gm, can be extracted from a closed loop gain measurement of the amplifier (if V_{comp} is an available pin)

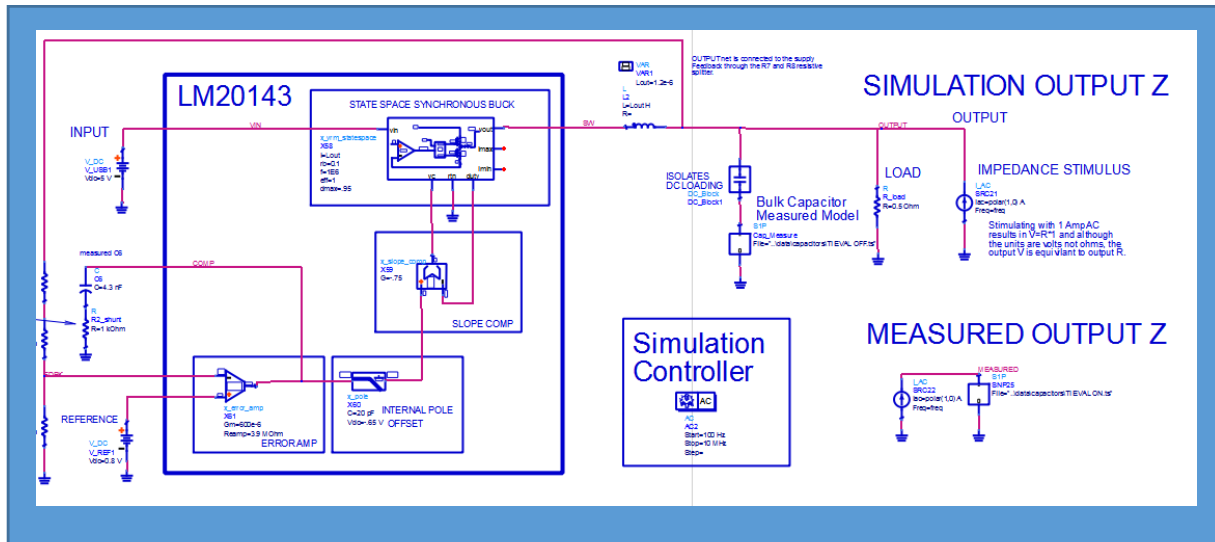


Statistical tolerances are extracted from measurements of several evaluation or characterization boards



Solving the System of Equations

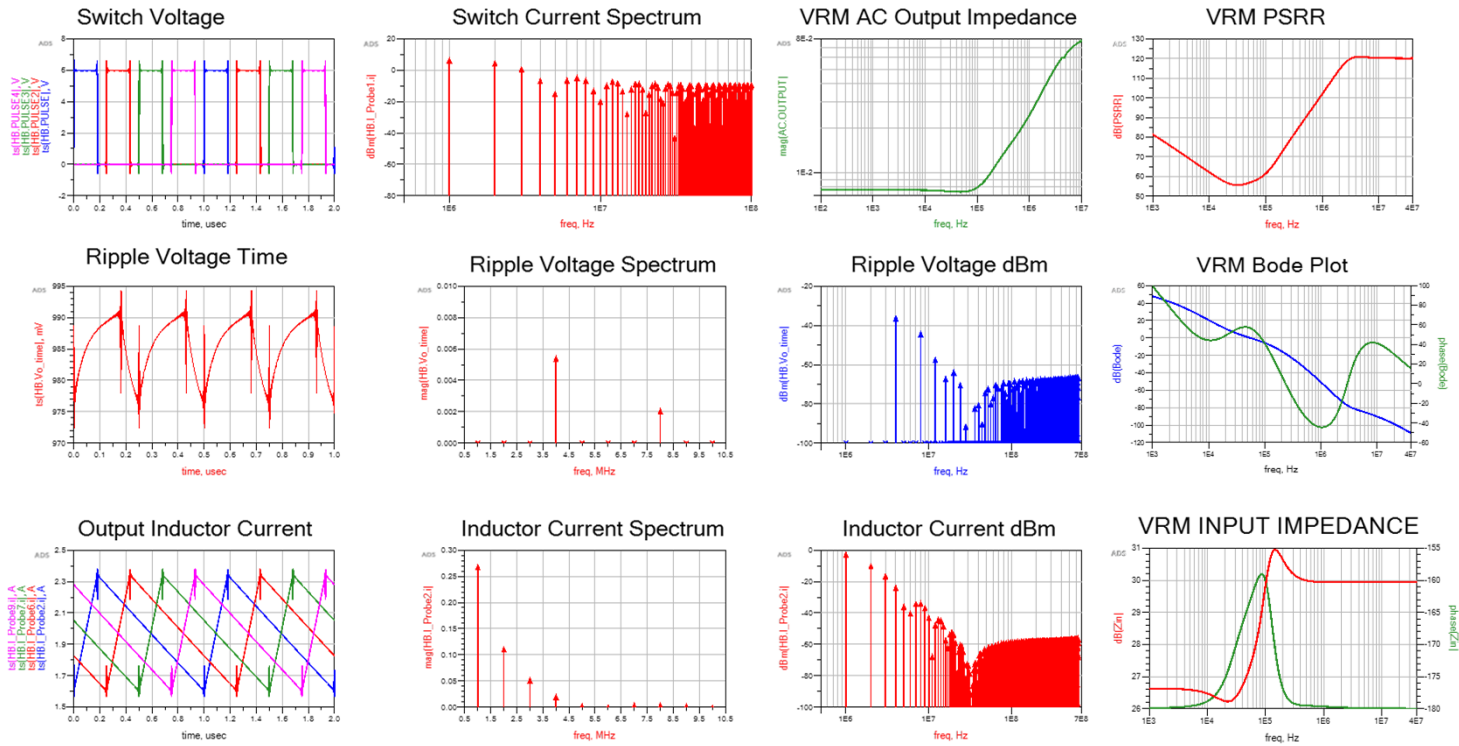
A few easy measurements and your favorite manual or automated multi-parameter equation solver provide a high fidelity model that supports optimization and worst case tolerance assessment



Var Eqn	VAR
	VAR1
	Vramp=1.3
	Fs=1E6
	Lo=1E-6
	Ri=0.1
	Vos=0.43



Results in an Accurate Simulation Model

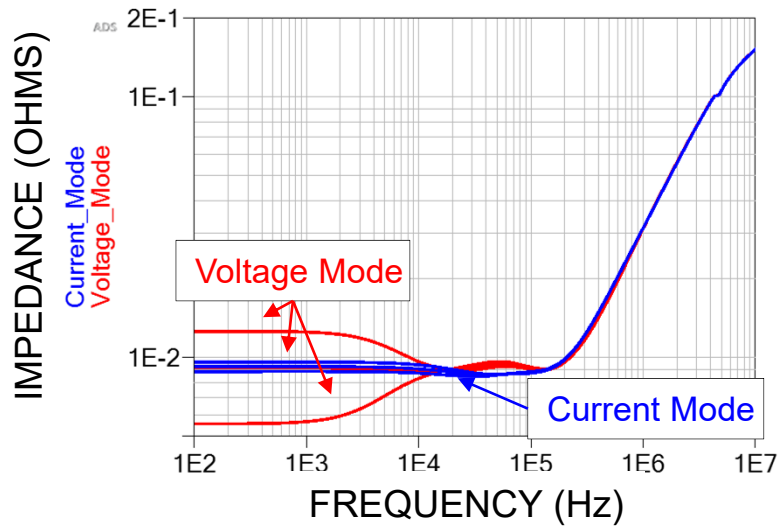


Current Mode is The Better Choice

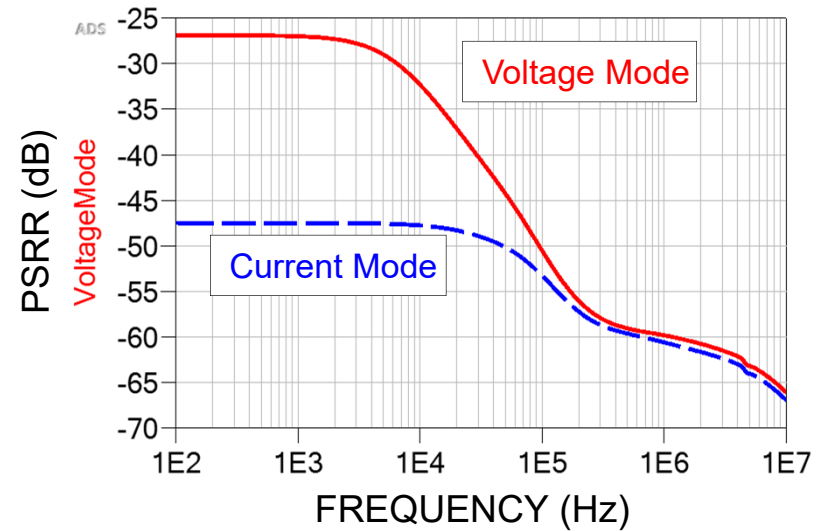
$$R_{out_CM} \cong \frac{R_i}{1 + A_v}$$

$$R_{out_VM} \cong \frac{DCR_{Lo} + R_{DSon_{bot}} + (R_{DSon_{top}} - R_{DSon_{bot}}) \cdot \frac{V_o}{V_{in}}}{1 + A_v \cdot \frac{V_{in}}{V_{ramp}}}$$

DCR_Lout +/- 45%



Power Supply Rejection Ratio (PSRR)

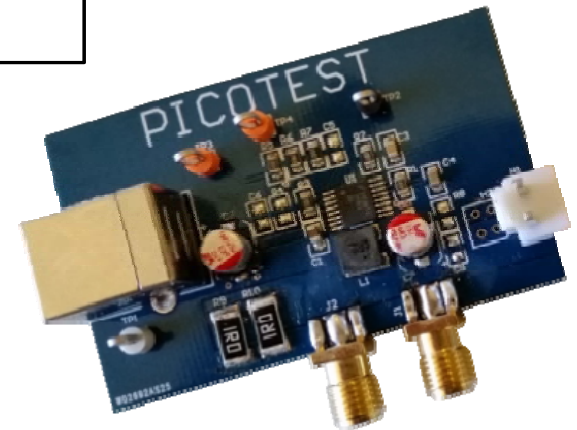
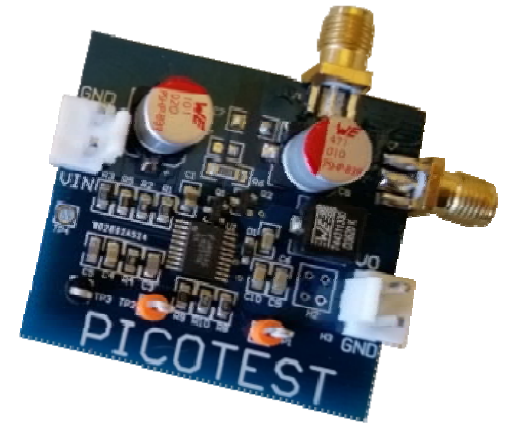


Small-Signal Figures of Merit

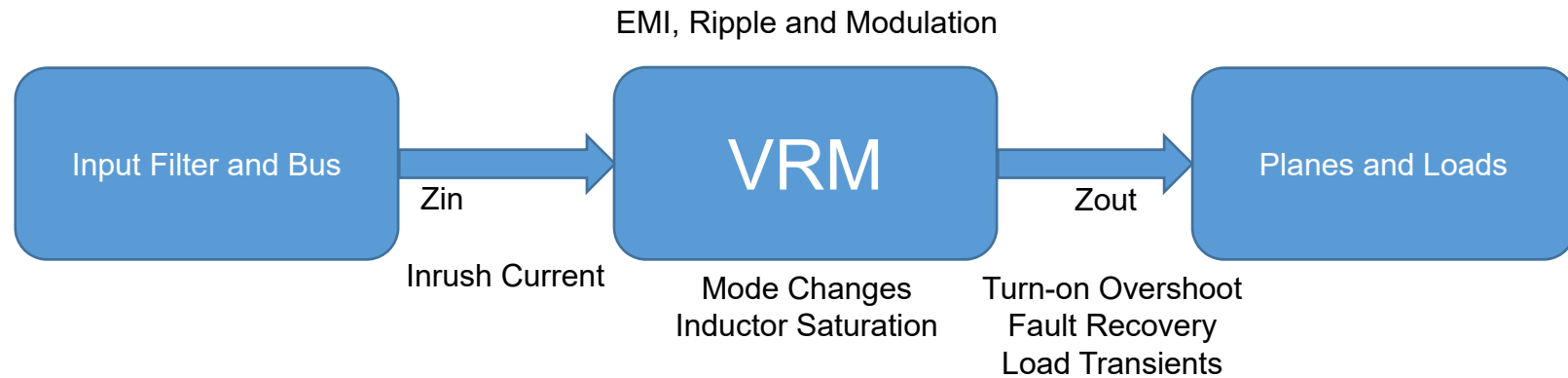
- *Topology (Current mode preferred)*
- *Controllable V_{ramp} (characterized is better)*
- *Compensation pin accessible*
- *R_i (external preferred over DCR sense)*
- *Flat output impedance*
- *EA GFS characterized including tolerance!*
- *EA gain bandwidth - higher is better*
- *Any internal poles defined*

It's often best to create your own MEASURABLE test board and acquire the data yourself

NOTE THAT FLAT IMPEDANCE AUTOMATICALLY ASSURES STABILITY 😊



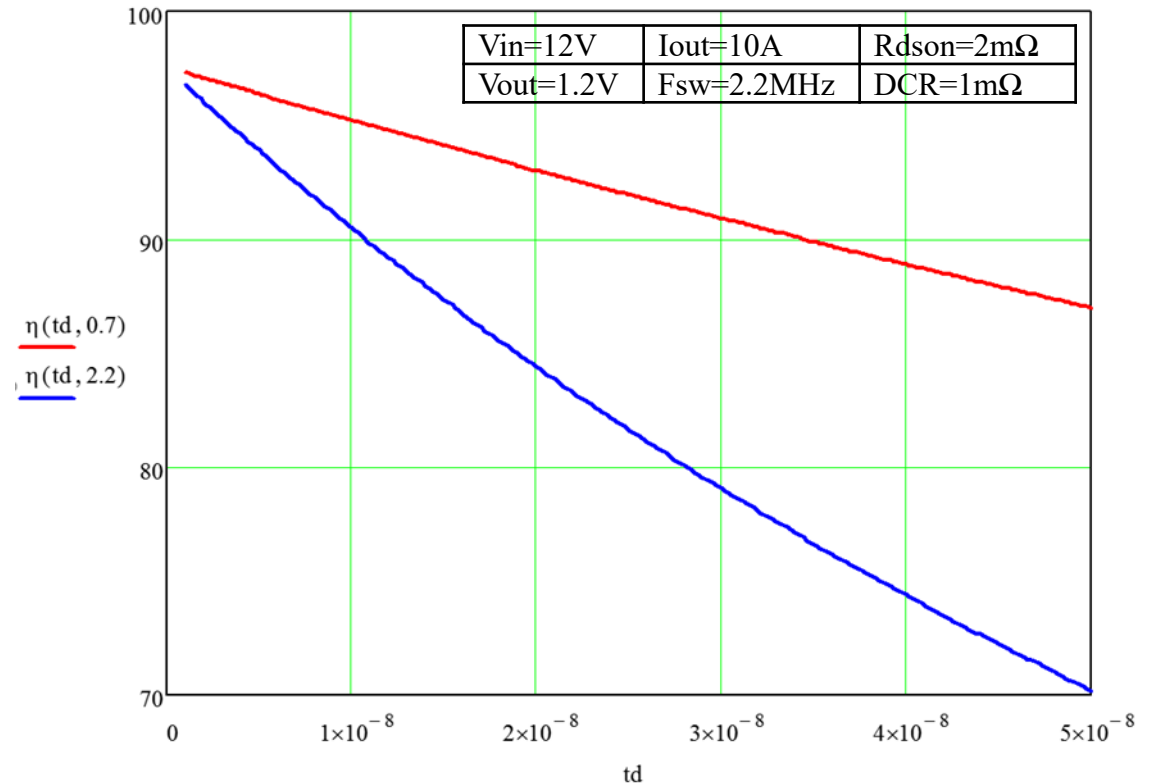
Additional Considerations



Power Losses

A significant portion of the total power loss is due to the switch
deadtime. This impact increases
rapidly with increasing switching
frequency and also with body
diode forward voltage

Most manufacturers only provide
typical deadtime, if that



$$P_{loss} = I_{out} \cdot \left(I_{out} \cdot R_{ds} + 2 \cdot F_{sw} \cdot V_f \cdot t_d \cdot \left(1 - \frac{I_{out} \cdot R_{ds}}{V_f} \right) + I_{out} \cdot DCR \right)$$

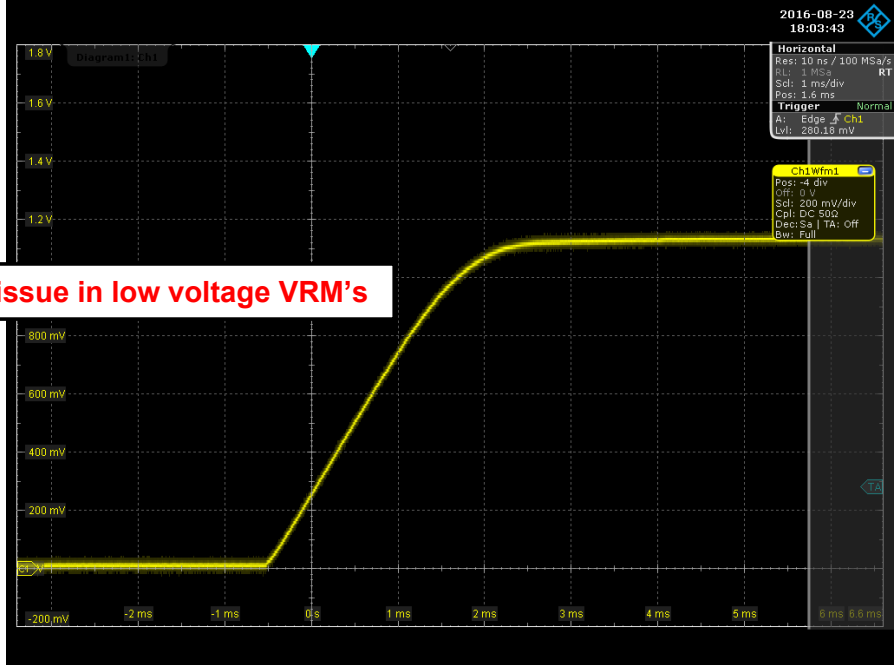


Turn-On and Fault Recovery

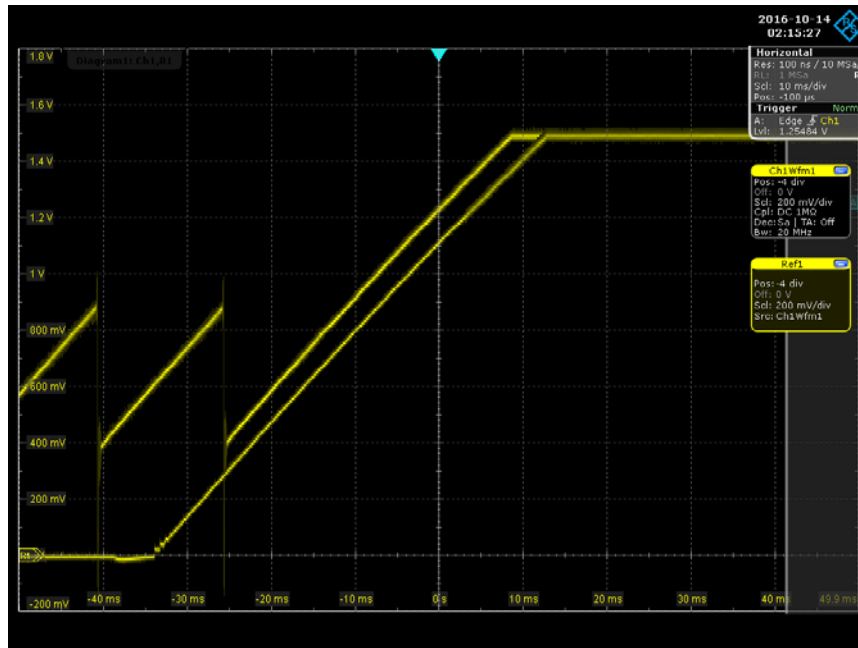


Turn on overshoot can be an issue in low voltage VRM's

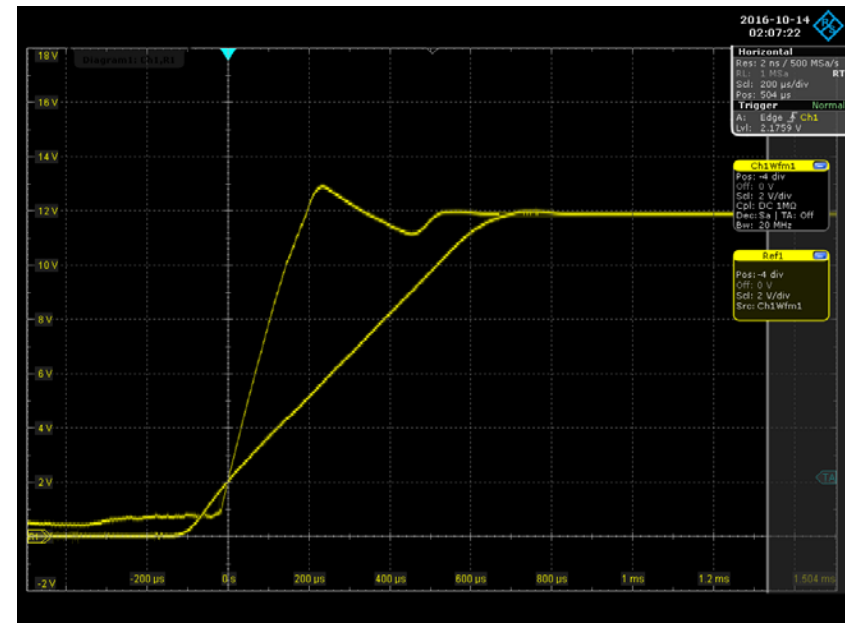
There is an associated inrush current due to the dv/dt on the bulk capacitors



Fault Recovery Often Bypasses Soft-Start



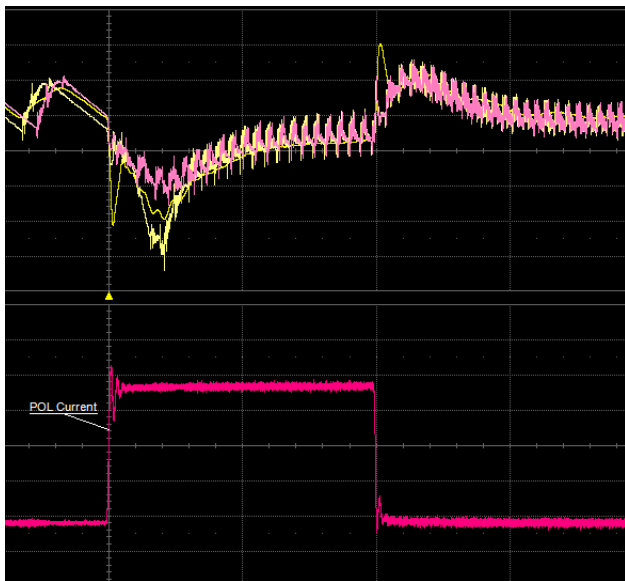
There is a larger inrush current due to the dv/dt on the bulk capacitors, as well as, the overshoot



Large Signal Response

$$\Delta V_o = \frac{\sqrt{C_o^2 \cdot V_o^2 + L_o \cdot C_o \cdot I_L^2 - L_o \cdot C_o \cdot dI_L^2}}{C_o} - V_o$$

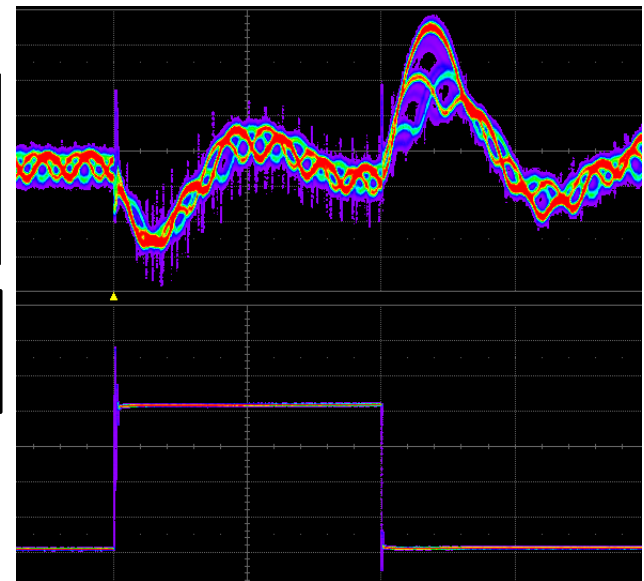
High duty cycle converters show large signal effects on the **increasing** current



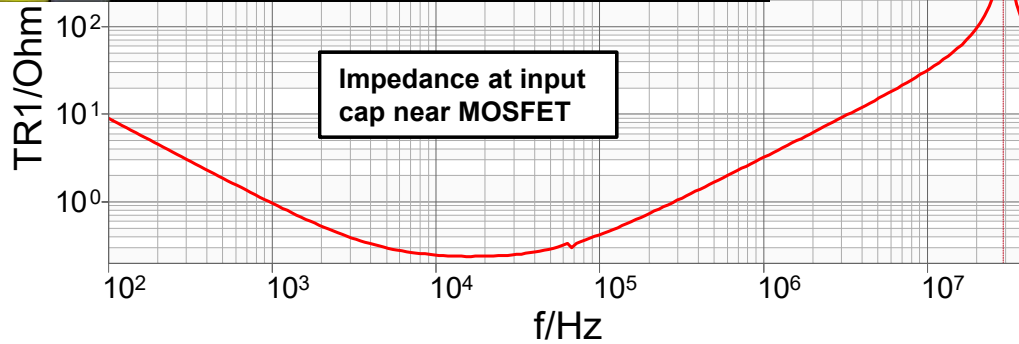
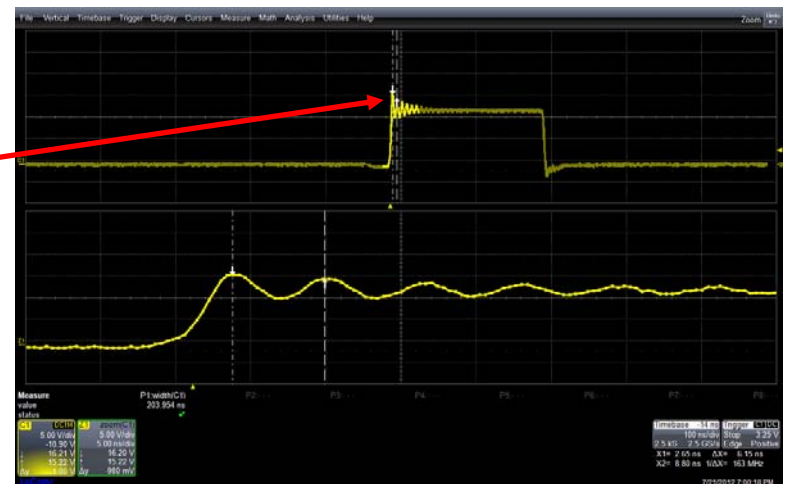
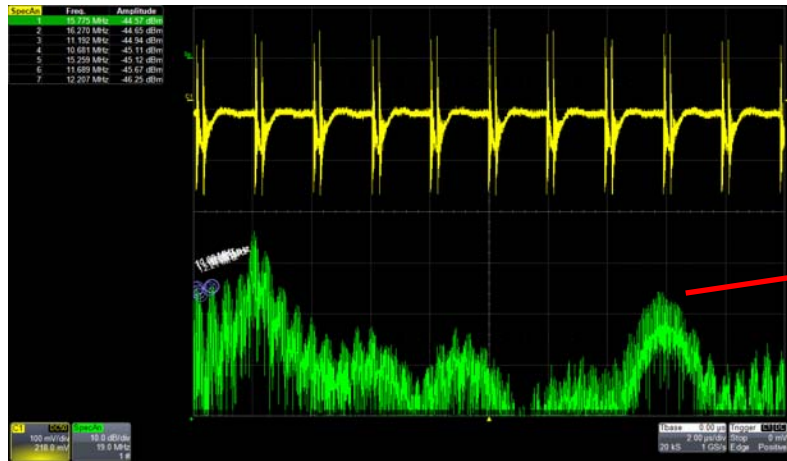
Step load response can be easily influenced by where in the switching cycle it occurs, so **do not average!** Use a digital filter or color persistence to highlight the responses if you need to

These measurements are performed with a 10ns, 15nF current injector so as not to interfere with the measurement

Low duty cycle converters show large signal effects on the **decreasing** current



EMI

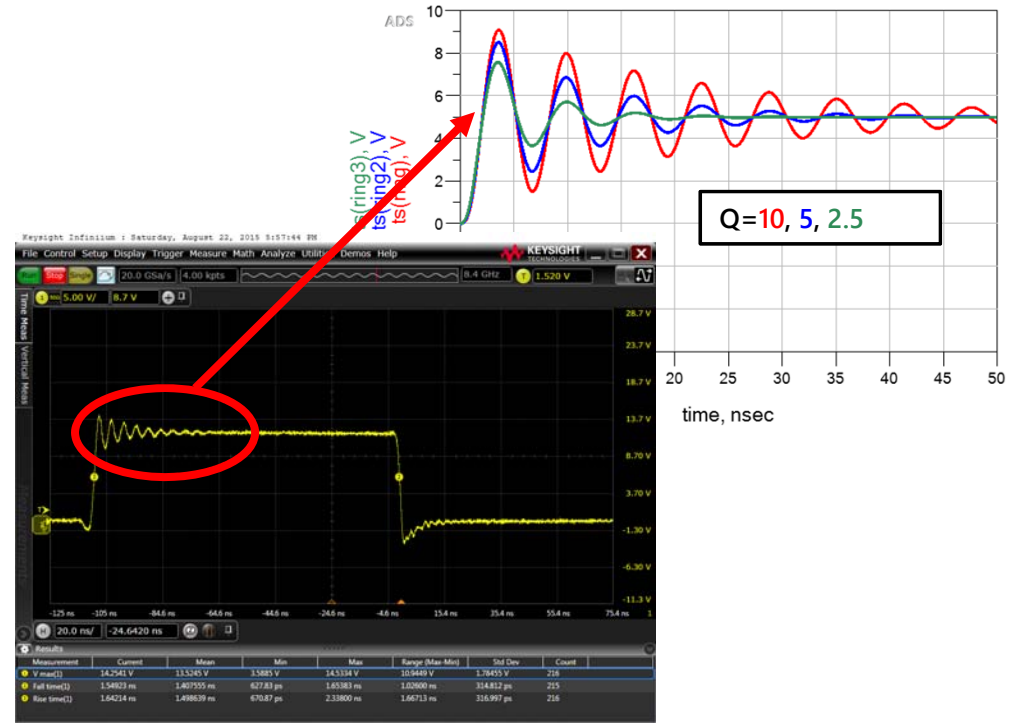
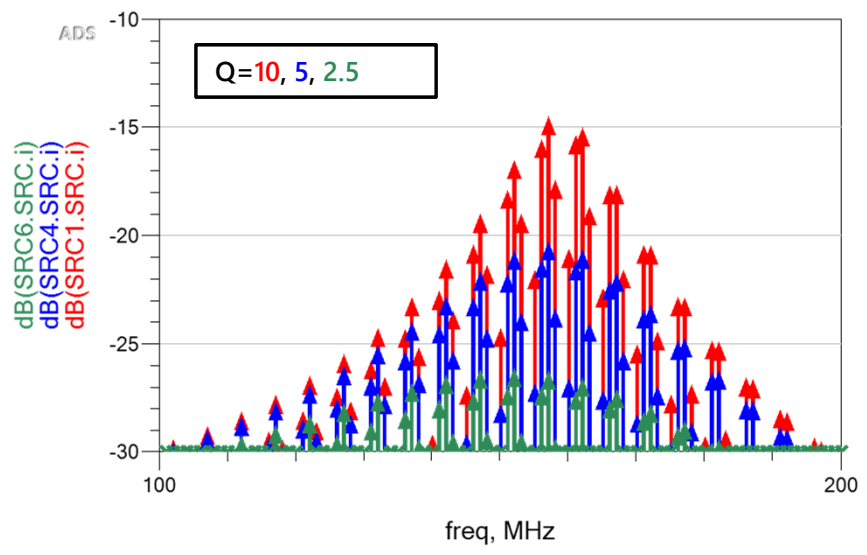


Resonant planes are often the source of EMI



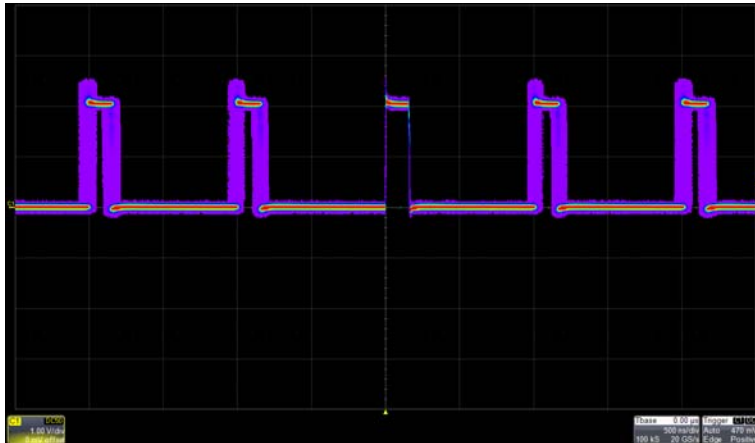
EMI Damping Effect

EMI is influenced mostly by the Q of the ring, not amplitude. So look for good damping

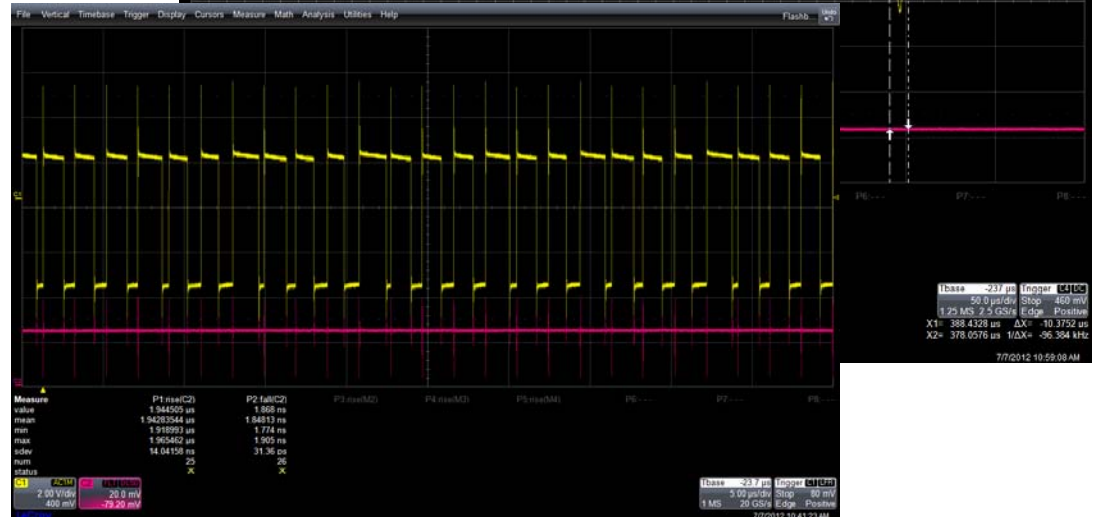


Modulated Noise Sources

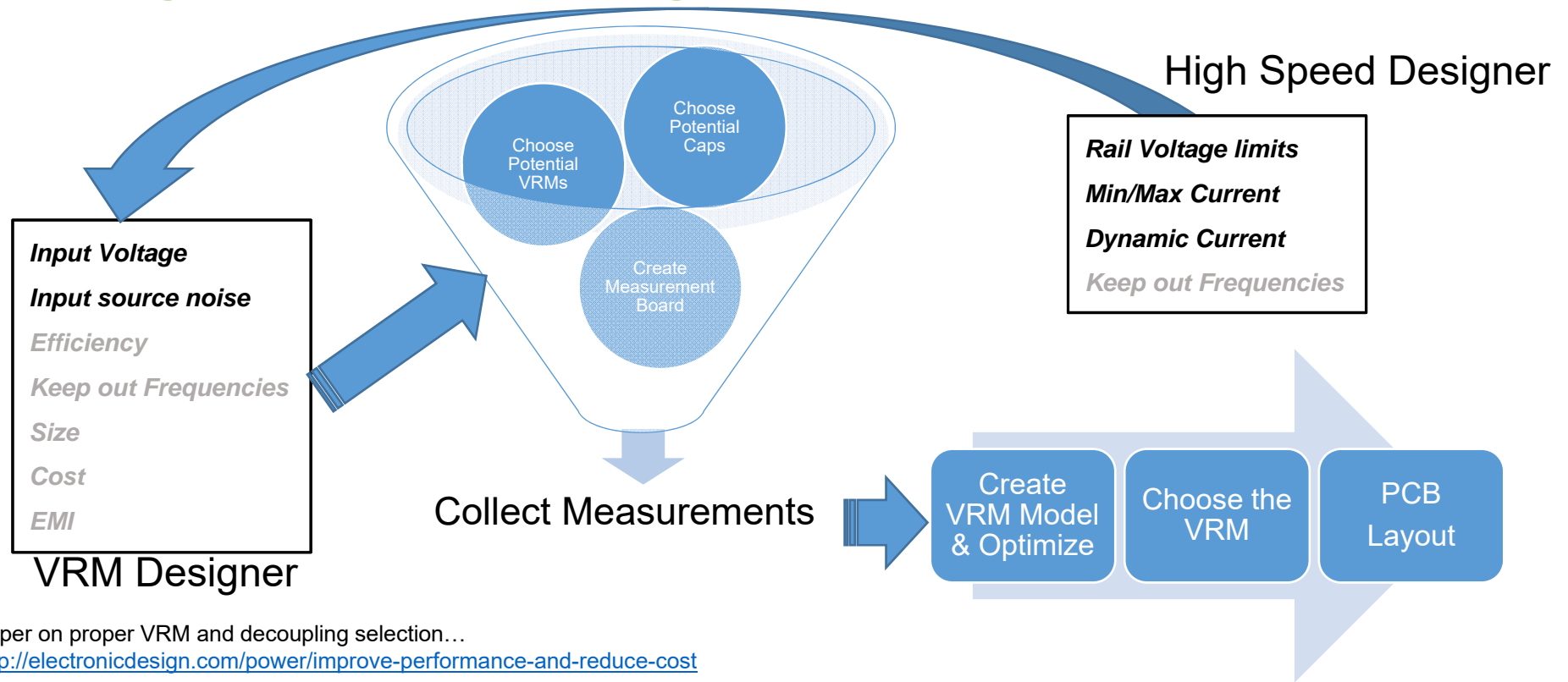
Some VRMs exhibit switching frequency modulation, which can be quite severe. In this example, the modulation introduces a time delay instability



Low frequency modulation can result in low frequency EMI which is extremely difficult to filter



Design Flow - Working Ends Towards the Middle



Paper on proper VRM and decoupling selection...

<http://electronicdesign.com/power/improve-performance-and-reduce-cost>



Conclusions

GET YOUR OWN DATA-PREFERABLY ON YOUR OWN CHARACTERIZATION BOARD

1. **Current mode control to optimize impedance**
2. **External slope compensation to optimize PSRR**
3. **External EA comp pin to acquire error amplifier data**
4. **Controllable Soft-Start (no turn-on overshoot)**

CAREFULLY LOOK FOR SIGNS OF AND CONSIDER IMPACTS OF:

- **Turn-On Overshoot**
- **Fault recovery (soft-start recovery)**
- **Large Signal transients**
- **Switching frequency modulation**
- **EMI plane resonances and switch resonant Q**
- **Chaotic behavior – parasitic SCR, saturation**
-

New Video - "How to Design for Power Integrity: Selecting a VRM", Keysight YouTube, 5/5/2016, <https://www.youtube.com/watch?v=ejAAplvIcR8&feature=youtu.be>

Articles

"Power Integrity: Measuring, Optimizing, and Troubleshooting Power Related Parameters in Electronics Systems", Steve Sandler, 7/29/2014, McGraw-Hill, ISBN: 0071830995,

"Three stability assessment methods every engineer should know about", Steve Sandler, 9/8/2016, <https://www.signalintegrityjournal.com/articles/192-three-stability-assessment-methods-every-engineer-should-know-about>

"Fix Poor Capacitor, Inductor, and DC/DC Converter Impedance Measurements", Steve Sandler, EEWeb, 10/2016, https://issuu.com/eeweb/docs/10-2016_modern_test_measure_1_pag

"This Misconception About Power Integrity Can Cost You Big", Steve Sandler, How2Power, 3/2016

"Improve Performance And Reduce Cost", Steve Sandler, 6/19/2014, Electronic Design, <http://electronicdesign.com/power/improve-performance-and-reduce-cost>

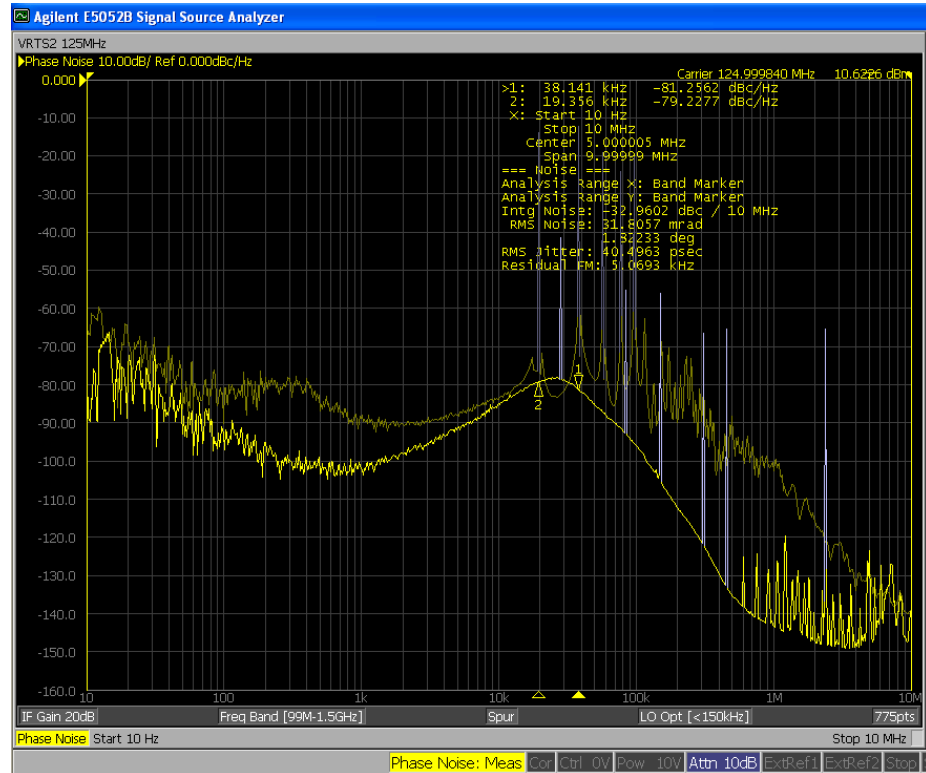
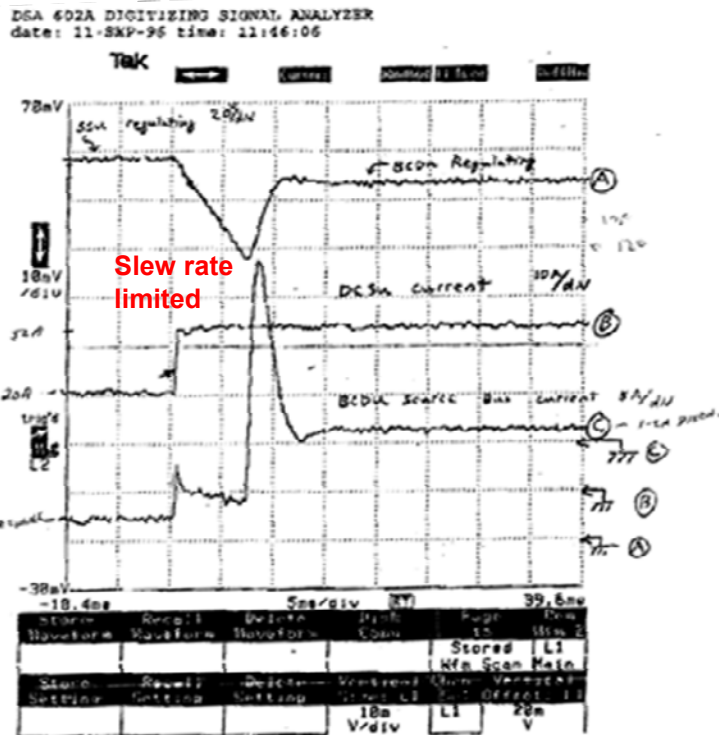
"How do I pick the best voltage regulator for my circuit?", Steve Sandler, 9/3/2013, Power Electronics, <http://powerelectronics.com/community/how-do-i-pick-best-voltage-regulator-my-circuit>

"Switch-Mode Power Supply Simulation: Designing with SPICE 3", Steve Sandler, 11/11/2005, McGraw-Hill, ISBN-10: 0071463267

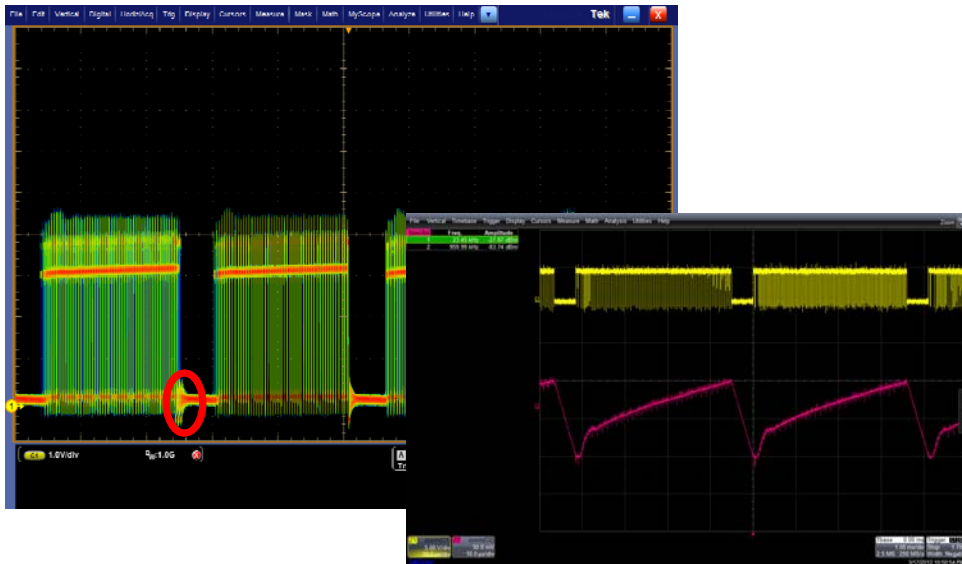


Mode Changes

While burst mode and pulse skipping modes can significantly improve efficiency, they can also result in time delay instabilities and increased noise. This clock phase noise plot shows the impact of burst mode



Other Noise Sources



Noise can conduct the substrate junction present in many controllers, which acts like a parasitic SCR, shutting down the VRM until the SCR releases. One result is greatly increased ripple at low frequency

Inductor saturation increases output ripple and EMI, but it can also impact small signal responses

