PICOTEST

# Are We Focused on the Wrong Voltage Reference Parameters?

The key to optimizing the performance of any circuit begins with a determination of the major performance criteria or "figures of merit" ("FOM"). Most engineers would likely consider the figures of merit (FOM) for a precision voltage reference to be:

- DC initial accuracy
- Temperature coefficient
- Thermal hysteresis
- Output noise
- Reverse current or headroom
- Output impedance

While these are arguably key characteristics, they may not be the most important and the performance in your circuit may often fall far short from the datasheet specifications.

A prerequisite to defining the mathematics of the reference is the understanding that there are different types of references. Specifically, there are series references and shunt references, as well as some that can be operated as either series or shunt devices. References are also either based on bandgap or buried zener elements. Independent of these differences, designers need to be aware of many of the performance characteristics. We can define the DC reference voltage output (Vo) to include the reference current (Io), reference DC output resistance (Ro), operating temperature (Temp), and hysteresis effect (Vhyst). The DC output voltage is defined in equation 1.

If we begin with the assumption that the characteristics above adequately define the reference performance, then the output voltage is the sum of the DC terms as shown in equation 1:

$$Vo = VR + \frac{\Delta VR}{\Delta VT} * (T - 25C) + \frac{\Delta VR}{\Delta Vin(or\ IReverse)} + \Delta VR + V_{hyst} \qquad \text{Eq. 1}$$

The resulting reference voltage output includes the initial accuracy of the reference, the temperature coefficient, sensitivity to input voltage or bias current (depending on the reference topology, aging and thermal hysteresis). While this might seem like a complete list, there are many more contributions to the output voltage.

- Thermocouple effects[i]
- Antenna effects
- Impacts of additional buffer amplifiers which are often used with ADC circuits
- Control loop stability
- Dynamic or AC load current variations
- Dynamic or AC input voltage ripple
- Capacitance loading of the reference

Thermocouple effects have been well documented[i] and can result in small changes in the output voltage, as well as independent noise contributions. Other sources of noise include antenna effects, such as from a switching regulator, which couples external noise into the reference output via long or poorly shielded traces. If we assume that the design carefully matches materials and eliminates thermal wind effects, as well as keeping traces short and shielded between ground planes then the thermocouple and thermal wind effects can be neglected along with the antenna effects.

The manufacturer generally provides measurements for the DC, temperature and noise characteristics of their devices. This leaves the dynamic and AC performance, which along with the internal control loop stability contribute to the output voltage variations.

**REF03 SPECIFICATIONS**

$V_{IN}$ = 15 V, −40°C ≤ $T_A$ ≤ +85°C, $I_{LOAD}$ = 0 mA, unless otherwise noted.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| OUTPUT VOLTAGE | $V_O$ | | 2.495 | 2.500 | 2.515 | V |
| OUTPUT ADJUSTMENT RANGE[1] | $\Delta V_{TRIM}$ | POT = 10 kΩ | ±6 | ±11 | | % |
| INITIAL ACCURACY | $V_{OERR}$ | | | | ±15 | mV |
| | | | | | ±0.6 | % |
| TEMPERATURE COEFFICIENT | $TCV_O$ | | | 10 | 50 | ppm/°C |
| LINE REGULATION[2] | $\Delta V_O/\Delta V_{IN}$ | $V_{IN}$ = 4.5 V to 33 V | | 20 | 50 | ppm/V |
| LOAD REGULATION[2] | $\Delta V_O/\Delta I_{LOAD}$ | $I_{LOAD}$ = 0 mA to 10 mA | | 60 | 100 | ppm/mA |
| DROPOUT VOLTAGE | $V_{DO}$ | | | | 2 | V |
| QUIESCENT CURRENT | $I_{IN}$ | | | 1.0 | 1.4 | mA |
| LOAD CURRENT | $I_{LOAD}$ | | | | | |
| Sourcing | | | | | 10 | mA |
| Sinking | | | | | −0.3 | mA |
| SHORT CIRCUIT TO GND | $I_{SC}$ | $V_O$ = 0 V | | 24 | | mA |
| VOLTAGE NOISE | $e_{NP-P}$ | 0.1 Hz to 10.0 Hz | | 6 | | µV p-p |
| LONG-TERM STABILITY[3] | $\Delta V_O$ | After 1000 hours of operation | | 50 | | ppm |

## APPLICATIONS INFORMATION

### BASIC REFERENCE APPLICATION

Figure 38 shows the basic configuration for any REF0x device. Input and output capacitance values can be tailored for performance, provided they follow the guidelines described in the Input and Output Capacitors section.

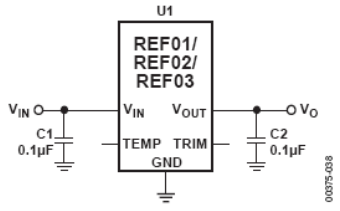


*Figure 38. Basic Reference Application*

Figure 1 Manufacturers application circuit and specifications for the Analog Devices REF03.

Several application notes are available that detail measuring voltage references including the measurement of reference output impedance, PSRR and noise[ii].

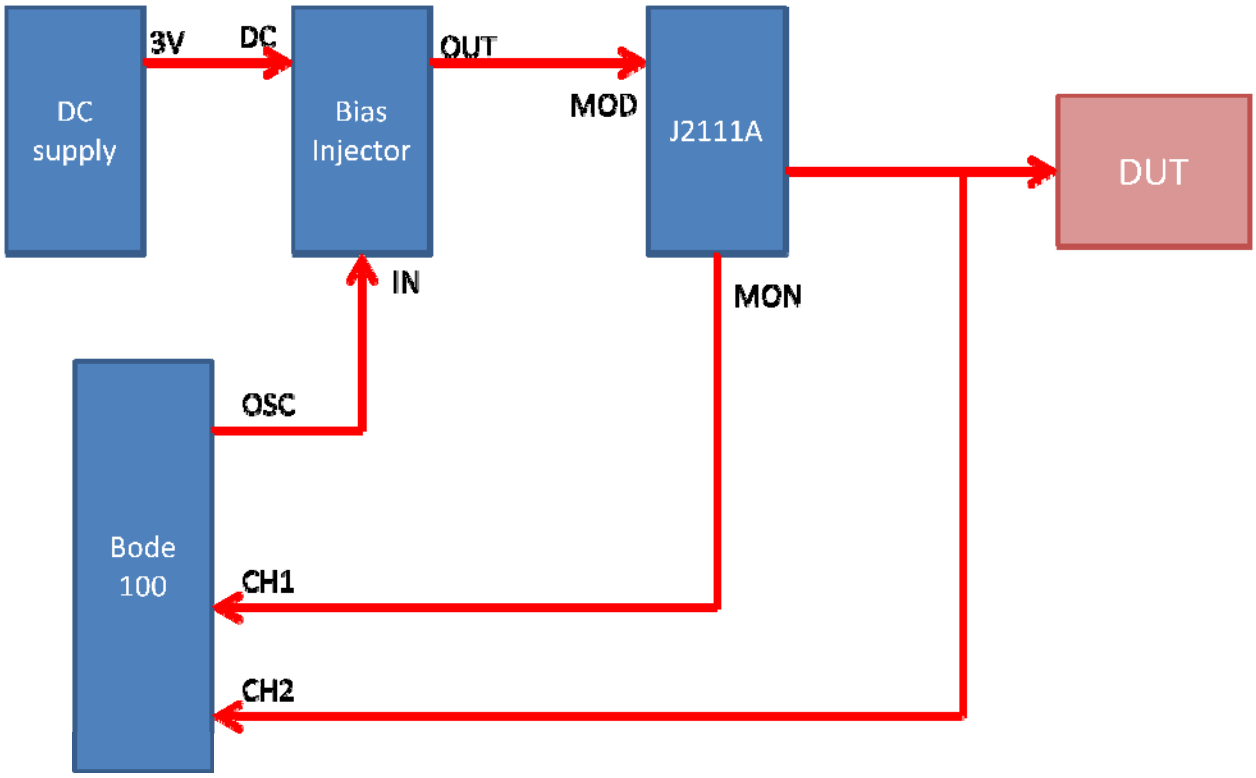


Figure 2 Block diagram of the output impedance measurement setup using the Picotest J2130 DC Bias injector, the J2111A Current Injector and the OMICRON Lab Bode 100 VNA.

A measurements of the output impedance of a REF03 voltage reference, is described in Figure 2 with the results shown in Figure 3. The measurement shows that while at low frequencies the reference output impedance is resistive, at higher frequencies, the output impedance appears inductive. The addition of a 0.1uF ceramic capacitor destabilizes the reference as can be seen from the 12.3 degree phase margin.

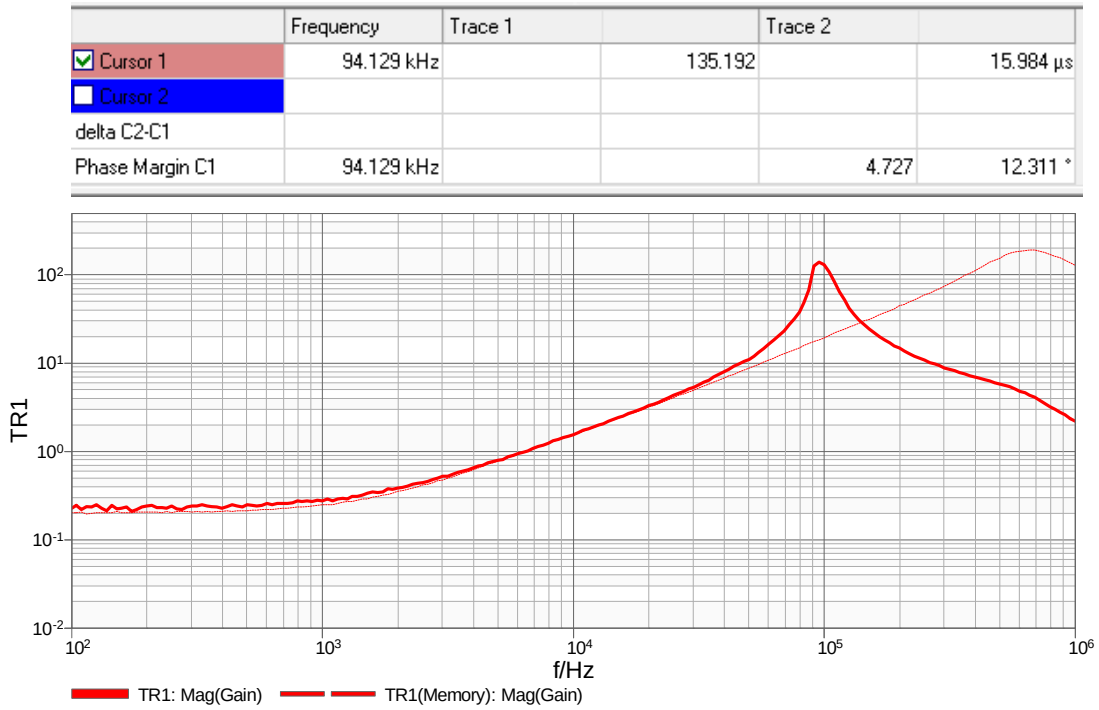


Figure 3 REF03 Output Impedance with (solid line) and without (dashed line) a 0.1uF X7R output capacitor, which is recommended by the manufacturer.

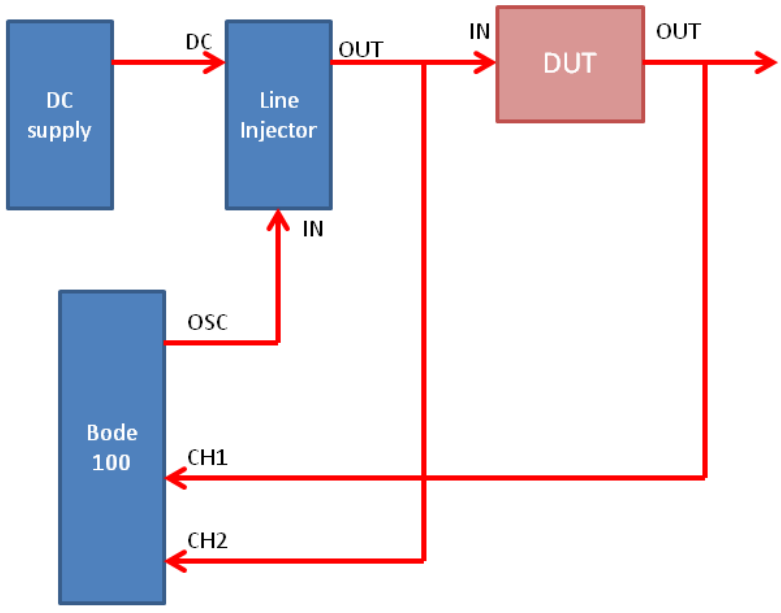


Figure 4 PSRR measurement test setup using the Picotest J2120 Line Injector.

The PSRR measurement can also be used to extract non-invasive phase margin. The result of this measurement, shown in Figure 4 indicates a phase margin of 10.2 Deg, which is close to the measurement obtained from the output impedance. The PSRR result is likely slightly more accurate as the signal resonance is somewhat less distorted.

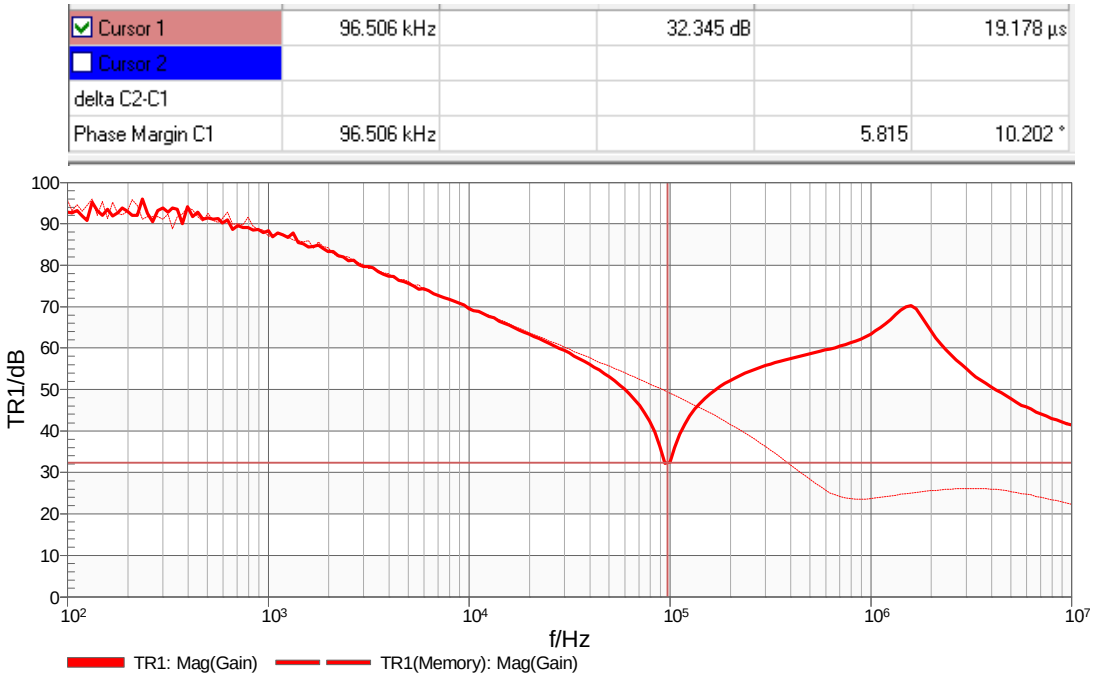


Figure 5 REF03 PSRR measurement with (solid line) and without (dashed line) a 0.1uF X7R capacitor. The phase margin is obtained directly from the Bode 100, using the PSRR measurement and the group delay, in much the same way as from the output impedance.

The typical specified DC line regulation from the datasheet is 20ppm, which converted to dB results in

$$20 \cdot \log\left[\frac{1}{\left(20 \cdot 10^{-6}\right)}\right] = 93.979 \text{ db}$$

This result is in excellent good agreement with the low frequency measured value seen in figure 5. Note that the specification is only provided for DC terms and not as a function of frequency.

Evaluating the impact of the control loop stability on the output noise we can show how input ripple to the reference or small load current variations at the regulator output can easily impact the reference performance. The typical output noise is listed in the manufacturers datasheet as 6uVpp.

The PSRR at94 kHz, with the recommended 0.1uF, capacitor is obtained from figure 5 as 32.345dB and multiplying this by the typical specified 6uVpp noise level results in:

$$6 \cdot 10^{-6} \cdot 10^{\frac{32.345}{20}} = 2.485 \times 10^{-4} \text{ uVpp}$$

This means that a 250uVpp 94 kHz noise signal at the reference input will result in an output noise signal that is equal to the typical specified reference output noise.

Similarly, the output impedance at 94 kHz is determined to be 135 Ohms from figure 3. Dividing the typical 6uVpp noise level by this output impedance we can determine the level of external load current variation required to equal the specified noise.

$$\frac{6 \cdot 10^{-6}}{135} = 4.444 \times 10^{-8} \text{ nApp}$$

This result indicates that a 94 kHz44nApp noise current, applied to the reference output, will equal the typical specified noise level.

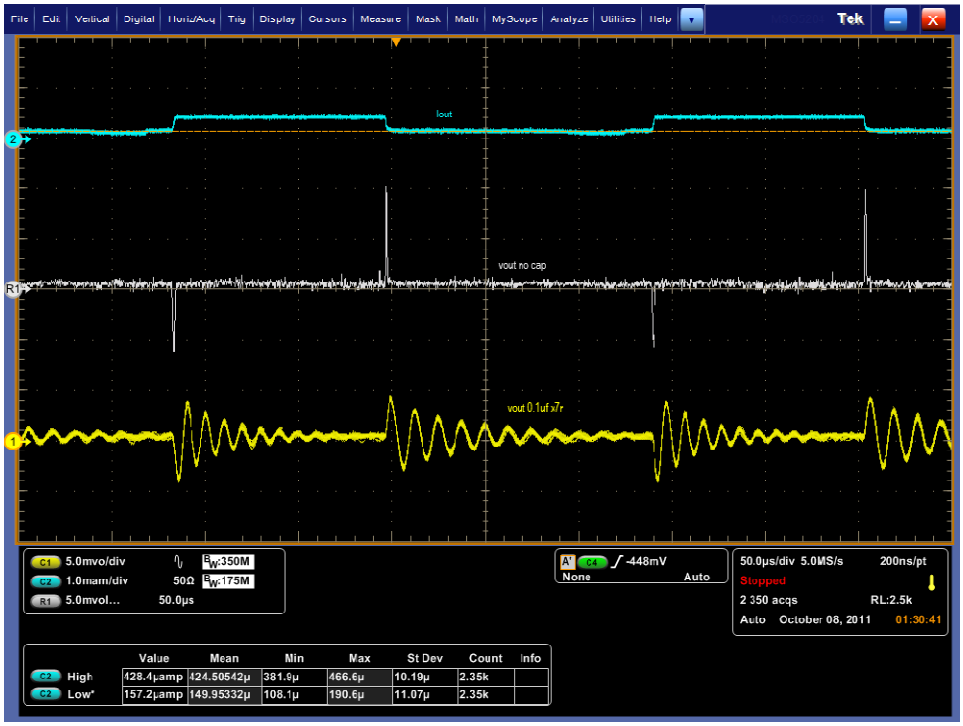


Figure 6 REF03 response to a step load (blue trace) with (lower yellow trace) and without (middle white trace) a 0.1uF X7R capacitor. Note that the current step is 1mA/Div or approximately 275uA step.

Figure 6 shows the step load response with and without the addition of a 0.1uF ceramic output capacitor. The severe ringing in the output response with the 0.1uF capacitor is representative of

the very poor phase margin, indicated in both the PSRR and output impedance measurements. This step load figure also shows that the ringing frequency is output current dependent as is the circuit Q. This can be determined since the responses are different at the low current level (150uA) than at the higher current level (425uA).

Comparing the results of the measurement with the specification it becomes clear that the data sheet supplied specification does little in the way of characterizing the AC or transient performance we can expect from the circuit. We can also conclude that using the REF03 with the manufacturer's recommended 0.1uF output capacitor significantly degrades the AC and transient performance of the part.

In order for engineers to predict the performance of references in real applications, and maybe more importantly, to assist in the selection of a reference, it seems that the FOM's need to be carefully re-evaluated.

In order to predict the performance of these reference voltage devices is it imperative that the manufacturers include an output impedance specification such as effective output inductance or alternatively Ohms/Hz AND a PSRR specification in dB-MHz. These specifications, in addition to the DC performance specifications, would allow the stability of the part to be assessed, as noted in a recent PET article[iii], while also allowing a better assessment of the PSRR.

As an example, it is currently possible for two reference devices to both specify a 90dB PSRR (as voltage stability or as a 120Hz data point), however, the parts may offer very different results at higher frequencies, where the larger concerns are. In the case of the REF03 with a 0.1uF capacitor the PSRR is only 32dB compared with 93dB at low frequency. This effect could be remedied by specifying PSRR in a similar way to gain bandwidth. The PSRR of 32dB in figure 5 with the 0.1uF capacitor at 94kHz is equivalent to a linear attenuation of approximately 40. Multiplying this by the 94kHz results in a PSRR specification of 3.76 MHz. Comparing this result to the curve without the capacitor from figure 5, the PSRR at 94kHz is 50dB, or a linear attenuation of 316. Multiplying this value by 94kHz results in 29. 7MHz. The degraded stability reduced this FOM by nearly a factor of 8. This recommended FOM also allows us to bound performance at other frequencies. For example, if we want the PSRR at 200kHz, we could divide the 29.7MHz by 200kHz and the result is 148. Converting this to dB results in 43dB PSRR, which is in good agreement with figure 5.

These improved FOM's would also benefit the manufacturers, as it gives the customers the justification for the increased cost for a part with real performance improvements. Lastly they would help increase the customer's chances for a first pass design success rate.

The recommended FOM's also apply to linear voltage regulators and LDOs, and in many cases also to opamps.

[i] "Linear Technology Application Note 82", November 1999, Linear Technology, http://www.linear.com

[ii] "Measuring the Output Impedance of Voltage References and Zener Diodes", Picotest Blog, http://www.picotest.com/blog
"A Simple Method to Determine ESR Requirements for Stable Regulators", Steve Sandler, Power Electronics Technology, August 4th 2011
http://powerelectronics.com/power_management/cad_cae/simple-method-determine-esr-requirements-stable-regulators-0811/

[iii]